Temperature Dependent Characterization of Ga_2O_3 MOSFETs with Spin-on-Glass Source/Drain Doping

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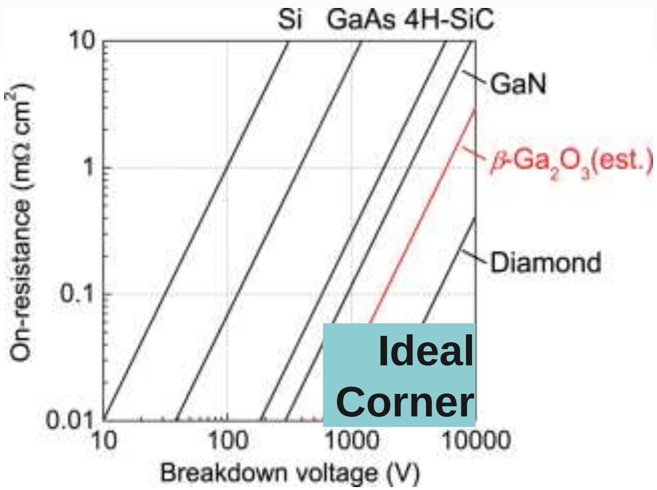
Motivation



*M. Higashiwaki et at, *Semicond. Sci. Technol.*, vol. 31, no. 3, p. 034001, (2016).

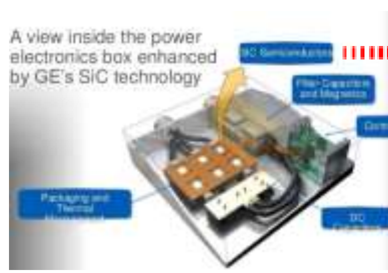
Key Applications of Power Electronics

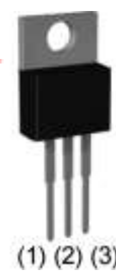
Automotive/HEV

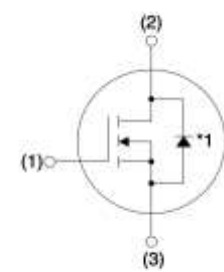
PV Inverters

Wind Turbines

Power Supply/UPS





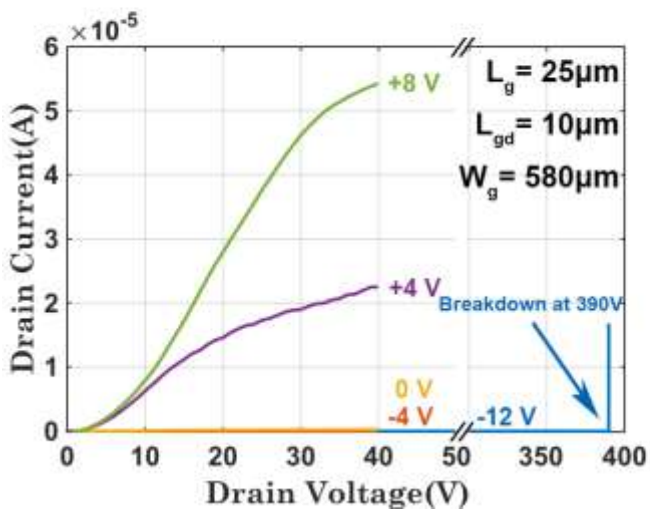


Power MOSFET

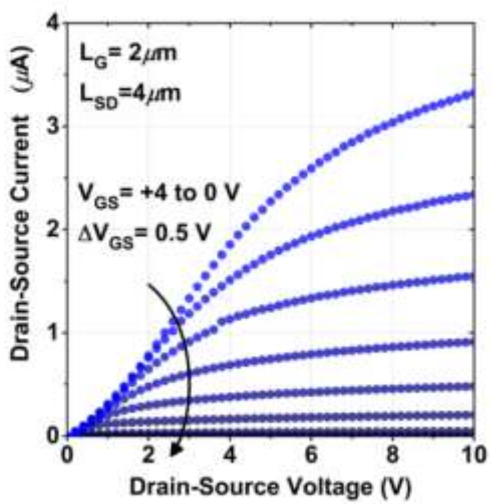
Source: General Electric Company, Getty Images, Infineon.

Ga_2O_3 MOSFETs

- First E-mode MOSFET on <2 × 10^{17}/cm^3 doped substrate
- Low current: high access resistance
- Non-linear IV behavior: Schottky like contact
- Lower 10^{17}/cm^3 is better for breakdown voltage



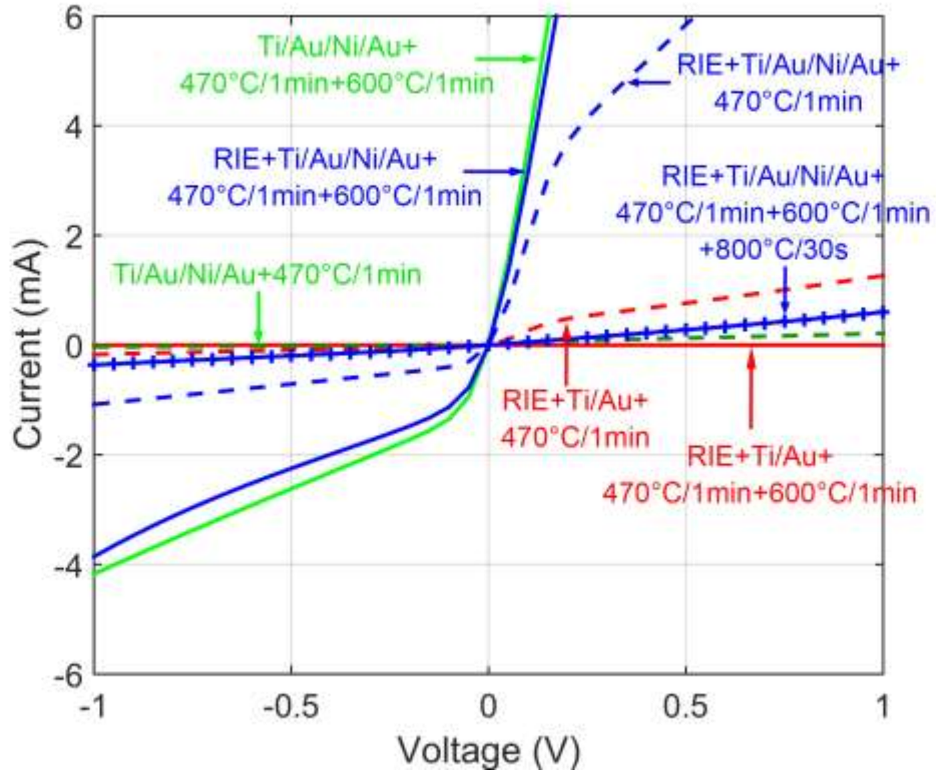
Zeng *et. al*, 2016 DRC.

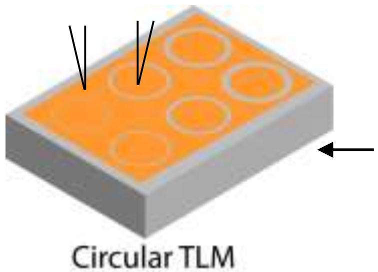


Chabak *et al. APL 109, 213501 (2016)*

Annealed Contacts to Ga_2O_3

- Annealed contacts: Ti/Au, Ti/Al/Ni/Au
- Better on highly doped Ga_2O_3 Low currents for $<2\times10^{17}/cm^3$ doping.
- I-V not perfectly linear: Schottky diode parallel with a resistor.
- Cannot extract ρ_c
- Degrade at high temperature



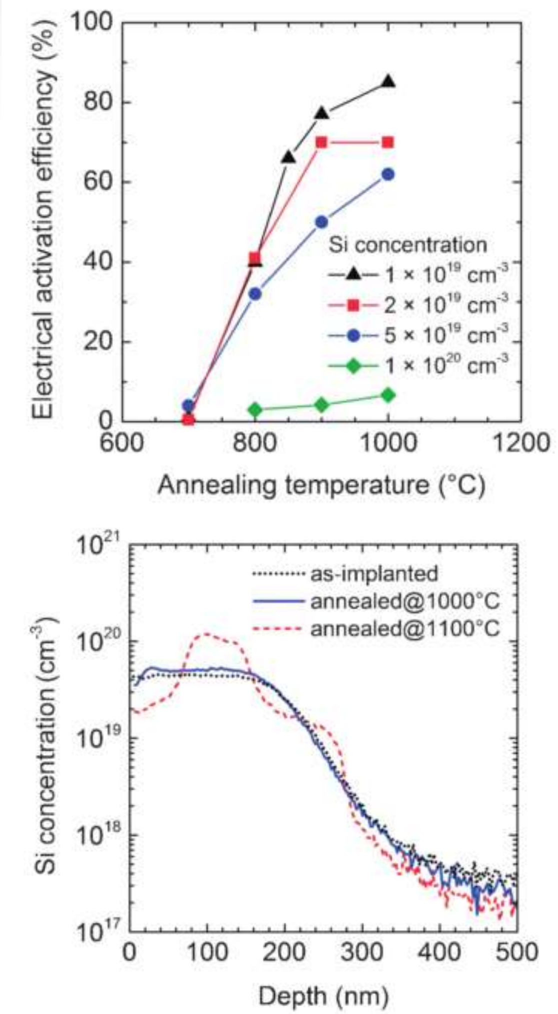


$2\times10^{17}/cm^3$ Sn Doped Substrate

Ion-implantation for Ohmics

- More control on the depth and profile of doping
- Good activation ratio
- Expensive
- Complex process
- High temperature long duration annealing(950 °C/30mins) *
- Difficult to incorporate at shallow depth(70nm RIE etch) *
- Ion-implantation induced damage

➢ An alternative method without these disadvantages: Spin-On-Glass(SOG) Doping Technique



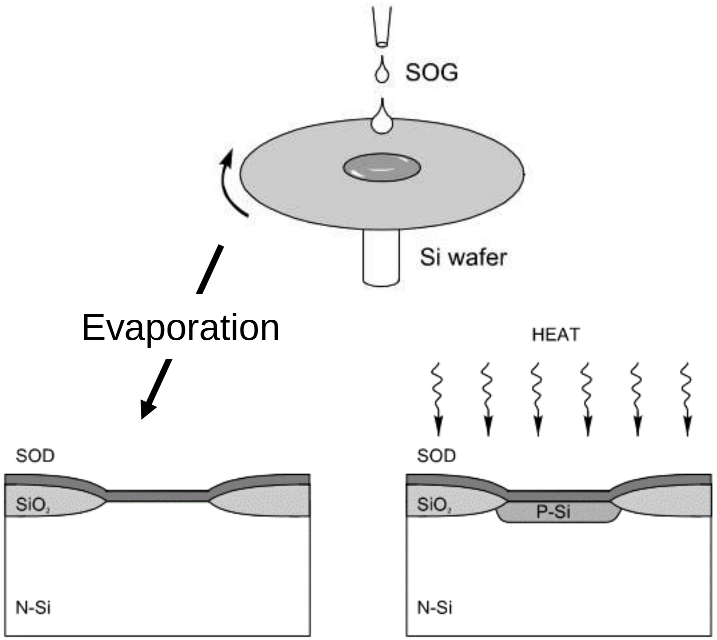
K. Sasaki et al. Appl. Phys. Express 6 (2013) 086502.

* WONG *et al*. IEEE EDL, VOL. 37, NO. 2, FEB 2016.

Spin-on-Glass (SOG) Doping Technique

- SOG: A glass layer that can be spin-coated onto the sample.
- **TEOS+Dopant Ion ➔**(Hydrolysis Reaction)➔ Solution of Dopant in Glass

- Quick and fast turn around process:
  - Spin coat, bake and anneal
- Highest doping at the surface
- Excellent for ohmic contact
- Less control on depth and profile

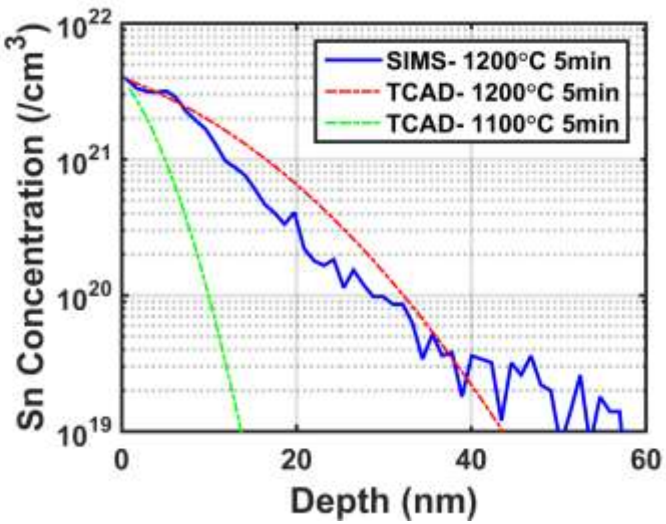


*T. Nguyen Nhu, *PhD Thesis*, Universiteit Twente, 1999.

Sn SOG Doping Experiment

- Sn is dopant in Ga_2O_3
- SOG Specifications (Dessert Silicon Inc):
  - Elements of Interest: Si, O, Sn
  - Key Element: Sn, 4×10^{21}/cm^3

- Doping Experiment:
  - Fe doped semi-insulating substrate
  - SOG Coats 170 nm at 3500 rpm
  - Drive-in RTA of 1100 °C/5 mins in N_2 ambient

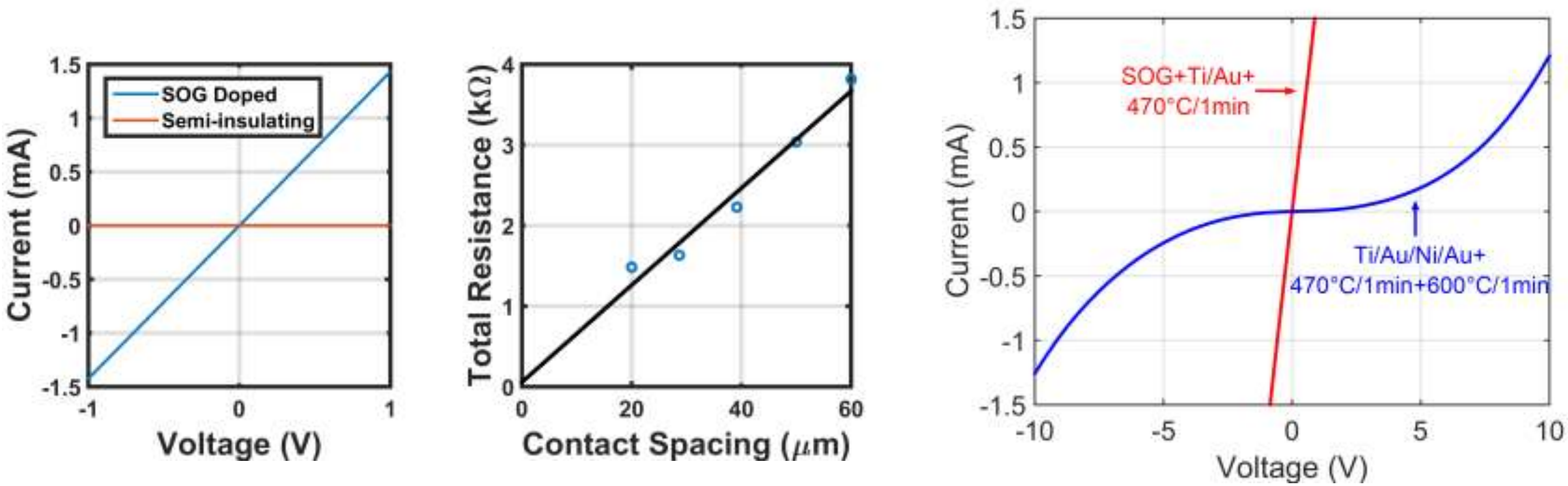


*SIMS data calibrated with Sn doped bulk sample.

$$D(T) = D_0 \exp(-\frac{D_E}{kT})$$

D_0= 0.8 and D_E= 4.2 eV

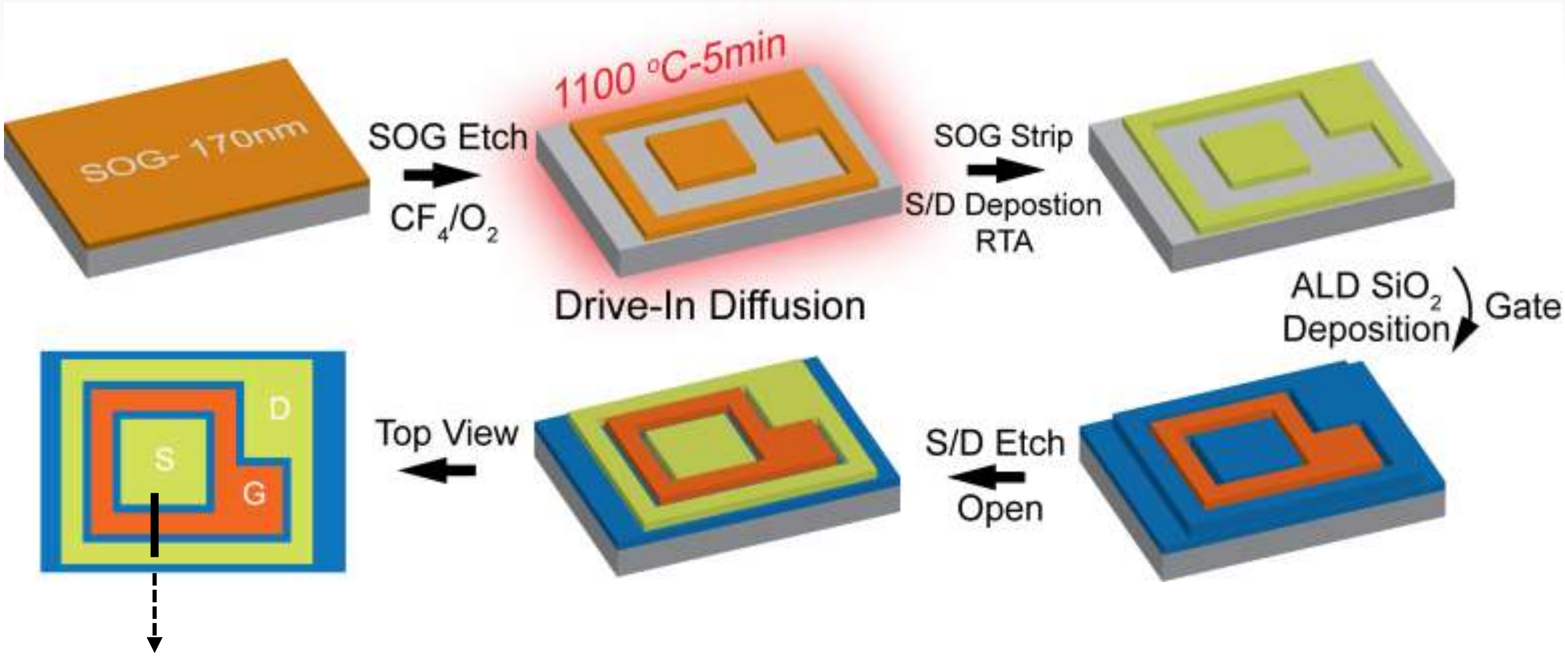
SOG Doped S/D Contact

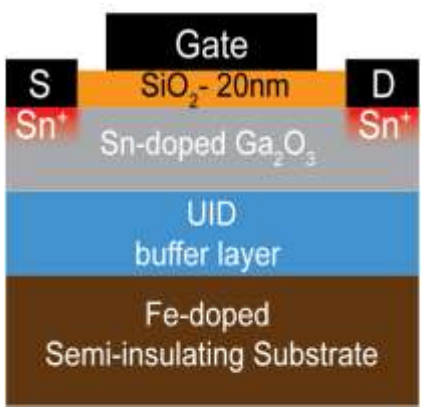


Credit: Abhishek Vaidya. (Labmate)

- 1100 °C/5mins drive-in diffusion: less than 20nm doping depth.
- ρ_c= 2.1$\pm$1.4$\times$10^{-5} Ω·cm^2.
- Higher current than Ti/Al/Ni/Au highest current.

SOG-FET Process Flow





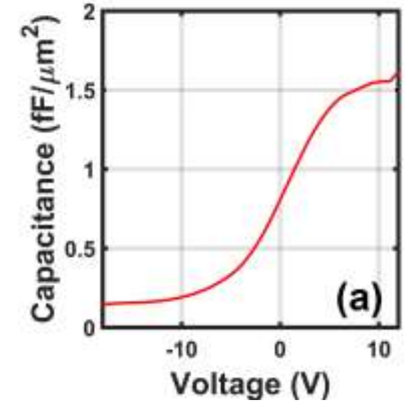
Cross-section schematic

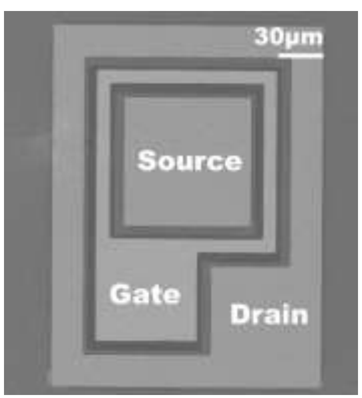
Device Specifications:

- 200 nm Sn-doped Ga_2O_3 epitaxial layer (grown by ozone MBE) on buffered Fe-doped semi-insulating substrate.
- Effective carrier concentration= $2 \times 10^{17}/cm^3$.
- 20nm gate SiO_2 by ALD.

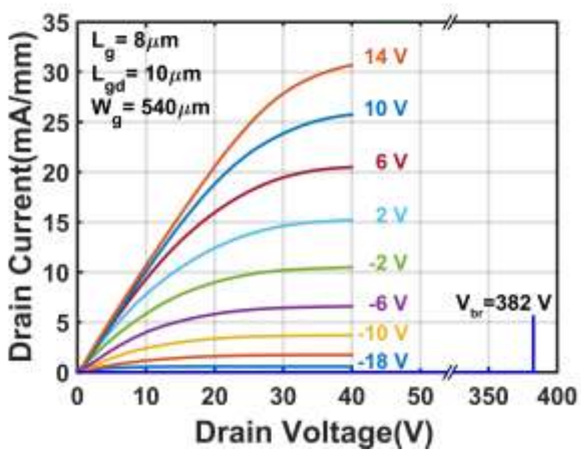
SOG S/D Doped MOSFET

- Much higher current compared to anneal contacts (DRC 2016)
- Peak current is 30 mA/mm
- Threshold voltage ~ -10V
- C-V characteristic

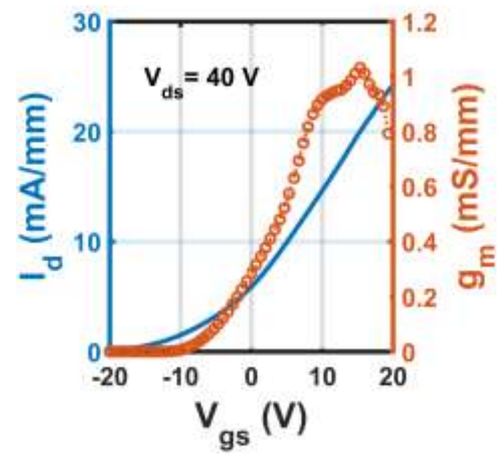




SEM image



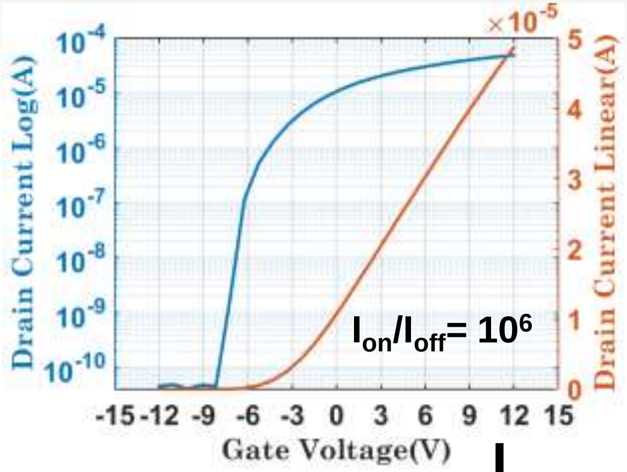
IV characteristic

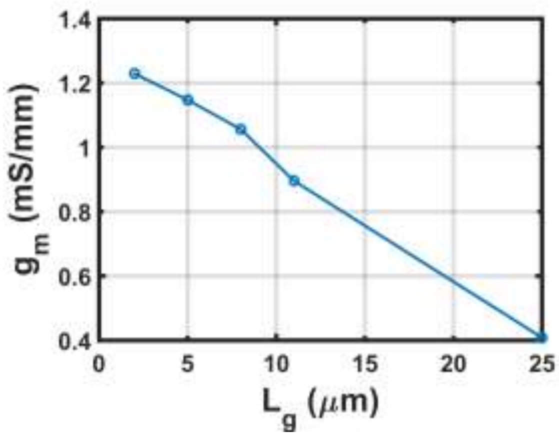


SOG S/D Doped MOSFET

- On/off ratio from **10^6** to **10^8** mainly due to increase of on current
- g_m(peak, max)= 1.23 mS/mm
- L_g scaling
- V_{br}= 382V (390V in 2016 DRC)

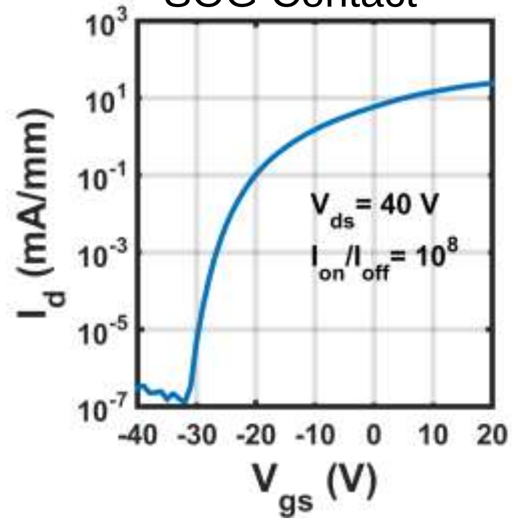
Annealed Contact



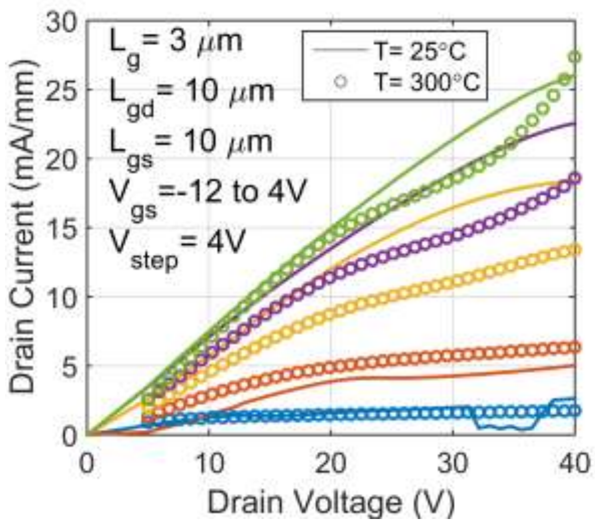


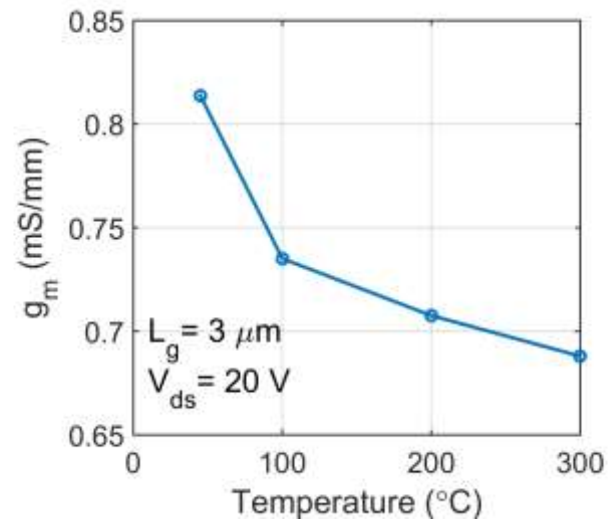
g_m(peak, max)= 1.23 mS/mm

SOG Contact



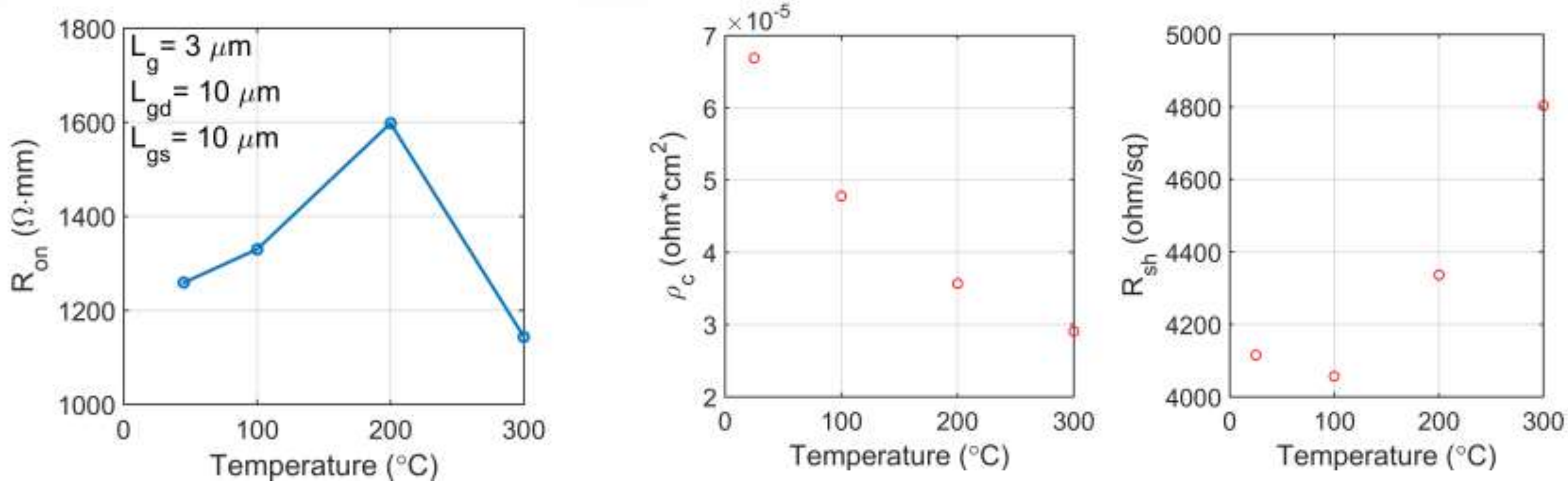
Temperature Dependent IV Characteristics





- Higher temperature, lower mobility, lower on current
- Higher temperature, more drain leakage, higher off current
    - Lower on/off ratio

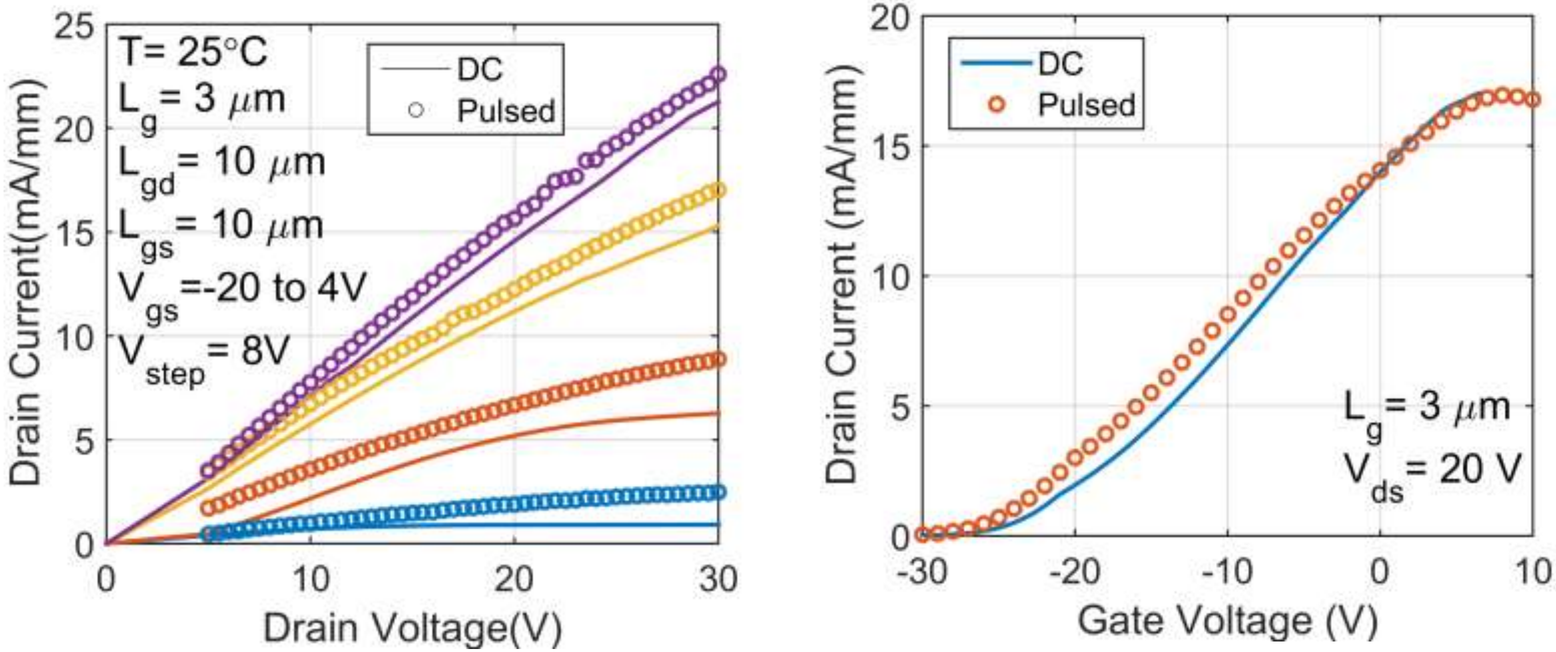
R_{ON} Temperature Dependence



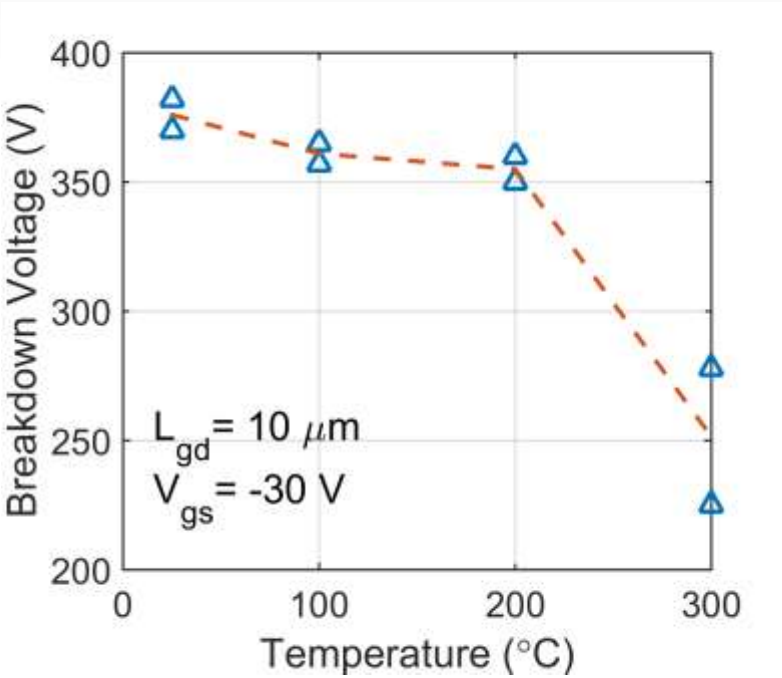
- $R_{ON} = R_C + R_{sh}$.
- T increases
  - R_C decreases
  - R_{sh} increase
- R_C still big enough to play a significant role in R_{ON}.

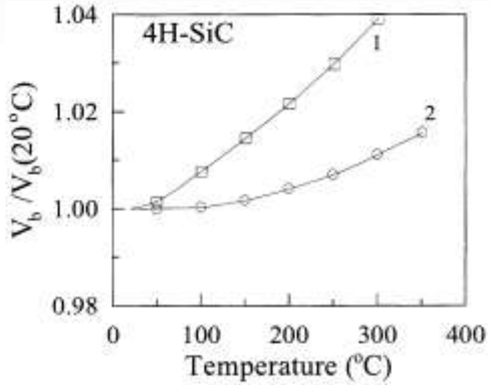
Pulsed IV

- Pulse width= 500 µs, period= 1000 ms (0.5% duty cycle).
- Pulse width is long: trap effects are not expected
- Increase in pulsed current: reduced self-heating



V_{br} Temperature Dependence





*Konstantinov et al. APL,73, 13 (1998), 1850

$$\alpha_p(4H-SiC) = 6.46\times10^6 - 1.07\times10^4 T\ *$$

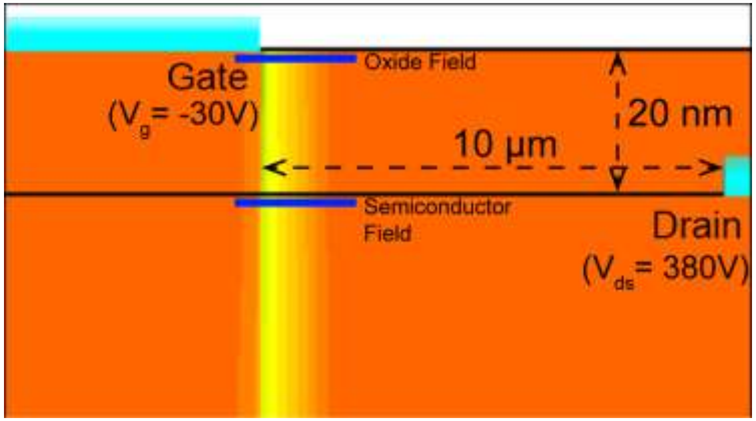
$$\alpha_n(GaN) = 4.42\times10^5 - 9.73\times10^2 T\ **$$

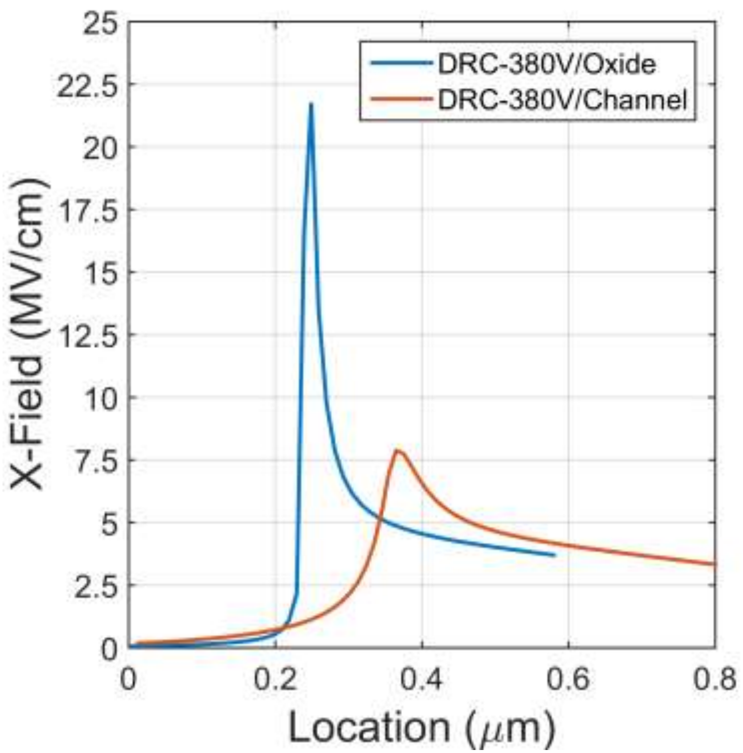
* B.J Baliga, *Fund. of Power Semiconductor Devices*, Springer, 2008.

** A.M Ozbek, *PhD Thesis*, NCSU, Raleigh, North Carolina, 2012.

- V_{br} decreases with increasing temperature (same with NICT report)
- **Not Impact ionization.**(T increases, phonon population increase)
- Breakdown in oxide?
- Related to Oxide defects, interface hot carrier generation, bulk defects.

Breakdown Simulation (TCAD)





- Peak field in Ga_2O_3~ 7.5 MV/cm, near breakdown.
- Field in the gate oxide >20 MV/cm, more likely to breakdown.
- Especially for defected gate oxide.

Conclusion

- SOG doping is a low cost method for ohmic contacts on low doping substrate.
- $\rho_c = 2.1 \pm 1.4 \times 10^{-5}\ \Omega \cdot cm^2$, $R_{sh} = 4.1\ k\Omega/\square$ on a 2E17 doped substrate.
- $I_{D(max)} = 30$ mA/mm , g_m(peak, max)= 1.23 mS/mm on SOG-FET
- T increase, g_m decreases, R_{ON} is lowest at 300°C.
- Breakdown is not impact ionization, more likely related to: Oxide defects, interface hot carrier generation, bulk defects.

Acknowledgement

- National Science Foundation (ECCS 1607833)
- Abhishek Vaidya and Susmita (Labmates)