QE Reduction due to Pixel Vignetting in CMOS Image Sensors

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ABSTRACT

CMOS image sensor designers take advantage of technology scaling either by reducing pixel size or by adding more transistors to the pixel. In both cases, the distance from the chip surface to the photodiode increases relative to the photodiode planar dimensions. As a result, light must travel through an increasingly deeper and narrower "tunnel" before it reaches the photodiode. This is especially problematic for light incident at oblique angles; the narrow tunnel walls cast a shadow on the photodiode, which in turn severely reduces its effective QE. We refer to this phenomenon as *pixel vignetting*. The paper presents experimental results from a 640×512 CMOS image sensor fabricated using a 0.35μ 4-layer metal CMOS process that shows significant QE reduction of up to 50% for off-axis relative to on-axis pixels. Using simple geometric models of the sensor and the imaging optics, we compare the QE for on and off-axis pixels. We find that our analysis results support the hypothesis that the experimentally observed QE reduction is indeed due to pixel vignetting. We show that pixel vignetting becomes more severe as CMOS technology scales, even for a 2-layer metal APS pixel. Finally, we briefly discuss several potential solutions to the pixel vignetting problem.

Keywords: CMOS imager, scaling, QE, vignetting

1. INTRODUCTION

CMOS image sensors hold out the promise of low power and camera-on-chip integration. However as CMOS technology scales, the performance of these sensors deteriorates due to the reduction in quantum efficiency (QE) and the increase in dark current.[1] It is well known that the QE of CMOS photodiodes decreases with technology scaling due to the reduction in junction depths and the increase in doping concentrations. In this paper, we investigate a less known but perhaps equally important reason for the reduction in QE. As CMOS technology scales, the distance from the surface of the chip to the photodiode, which we denote by h, increases relative to the photodiode lateral dimension w. Sensor designers take advantage of technology scaling either by reducing pixel size or by adding more transistors to the pixel.[2] Since the thickness of the interconnect layers scales slower than the planar dimensions,[3] reducing the photodiode size increases the ratio h/w. Alternately, adding more interconnect layers to the pixel without reducing its size also increases h/w. As a result, light must travel through an increasingly deeper and/or narrower "tunnel" before reaching the photodiode surface. This is especially problematic for light incident at an oblique angle. In this case, the tunnel walls cast a shadow on the photodiode area. We denote this phenomenon as *pixel vignetting*, since it is similar to vignetting in optical systems.[4] Because pixel vignetting reduces the light incident at the photodiode surface, it can severely reduce QE. Figure 1 plots h/w for a 2-layer metal CMOS photodiode active pixel sensor (APS)[5] and a 4-layer metal digital pixel sensor (DPS)[2] assuming a 30% fill factor as technology scales. Note that h/w for both APS and DPS keeps increasing as technology scales.

The remainder of this paper is organized as follows. In section 2, we report experimental results obtained from a CMOS 640×512 DPS[6] that demonstrate the QE reduction as a function of the angle of incidence of illumination . We first report the measured reduction of QE as a function of the angle of incident collimated light. Next, we report results comparing the QE for on and off-axis pixels using an imaging lens. In section 3, we derive the QE reduction due to pixel vignetting using simple geometric models of the sensor and the imaging optics. We find that our analysis results support the hypothesis that the measured QE reduction is indeed due to pixel vignetting. We then use these models to estimate this reduction as CMOS technology scales. Finally in the conclusion, we briefly discuss several solutions to the pixel vignetting problem.

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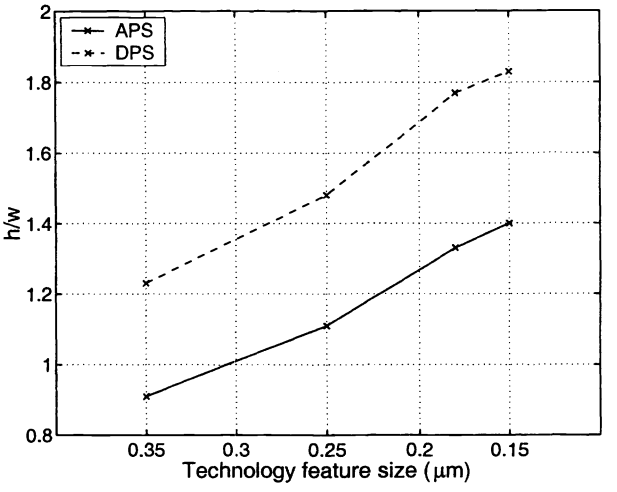

Figure 1. The h/w ratio for pixels of a 2-layer metal CMOS photodiode active pixel sensor (APS) and a 4-layer metal digital pixel sensor (DPS) assuming a 30% fill factor as technology scales.

2. EXPERIMENTAL SETUP AND RESULTS

In this section, we report experimental results obtained from a 640 × 512 CMOS image sensor that demonstrate the QE reduction due to pixel vignetting. We perform two experiments. The purpose of the first is to demonstrate that pixel vignetting is a serious cause of QE reduction, while the purpose of the second is to show the effect of pixel vignetting in a more realistic image capture setting. In the first experiment, we illuminate the sensor by a uniform quasi-plane wave and measure the average pixel response as a function of incidence angle. In the second experiment, we uniformly illuminate a quasi-Lambertian surface and measure the on and off-axis pixel responses to the uniform image field using imaging optics.

2.1. The 640 × 512 Sensor Characteristics

The 640 × 512 CMOS DPS used in the experiments features a Nyquist rate pixel-level ADC.[6] Each 2 × 2 pixel block shares a single ADC circuit comprising a comparator and a one-bit latch. The readout is done one pixel quadrant at a time. The sensor is fabricated using a standard 0.35μ, 4-layer metal, 1-layer poly, nwell digital CMOS process. The pixel consists of a nwell/psub photodiode and 5.5 transistors. It uses 3 layers of metal for interconnects and the 4th metal layer as a light shield. The pixel area is 10.5μm×10.5μm of which 29% is exposed to light. The fill factor, *i.e.* the fraction of pixel area occupied by the photodiode, is 8%. The layout of a single 2 × 2 pixel block sharing one ADC is shown in Figure 2. Note that the layout of the photodiodes is not completely symmetrical. As we show later, this causes a different response for each quadrant. Figure 3(a) is a top-view SEM image of the sensor showing the square openings through the 4th metal layer. Each square opening measures 5.5μm on a side. Figure 3(b) is the cross-section diagram of a DPS pixel with the 4th metal layer acting as a light shield.

2.2. Uniform Quasi-Plane Wave Experiment

In this experiment, we illuminate the sensor by a uniform quasi-plane wave (UQPW). This generates a uniform irradiance field at the surface of the sensor array and should produce identical responses from all pixels, except for noise and FPN. We perform the experiment for different angles of incidence and calculate the average pixel response at each angle.

Our experimental setup is shown in Figure 4. It consists of a stabilized white light source, a fiber light guide, a beam collimator and the CMOS sensor mounted on a rotation stage.

The uniform quasi-plane wave is generated by coupling the light from the stabilized white light source into a fiber light guide that leads it into a beam collimator. The board with the sensor is vertically mounted

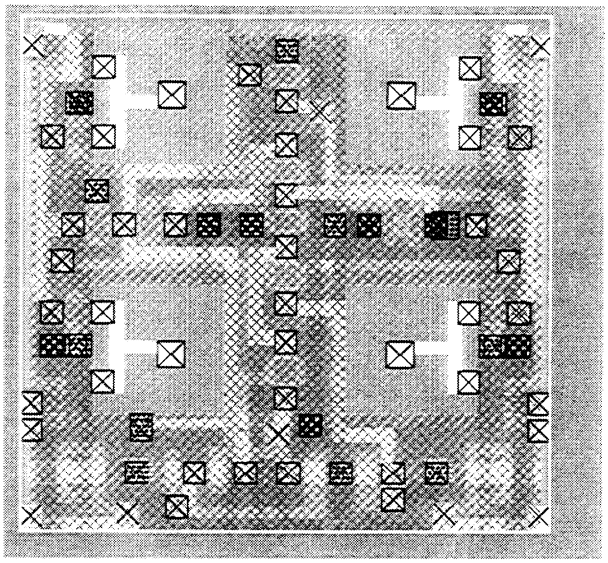

Figure 2. Layout of a 2 × 2 pixel block sharing one ADC. The transistors are shielded by the 4th metal layer.

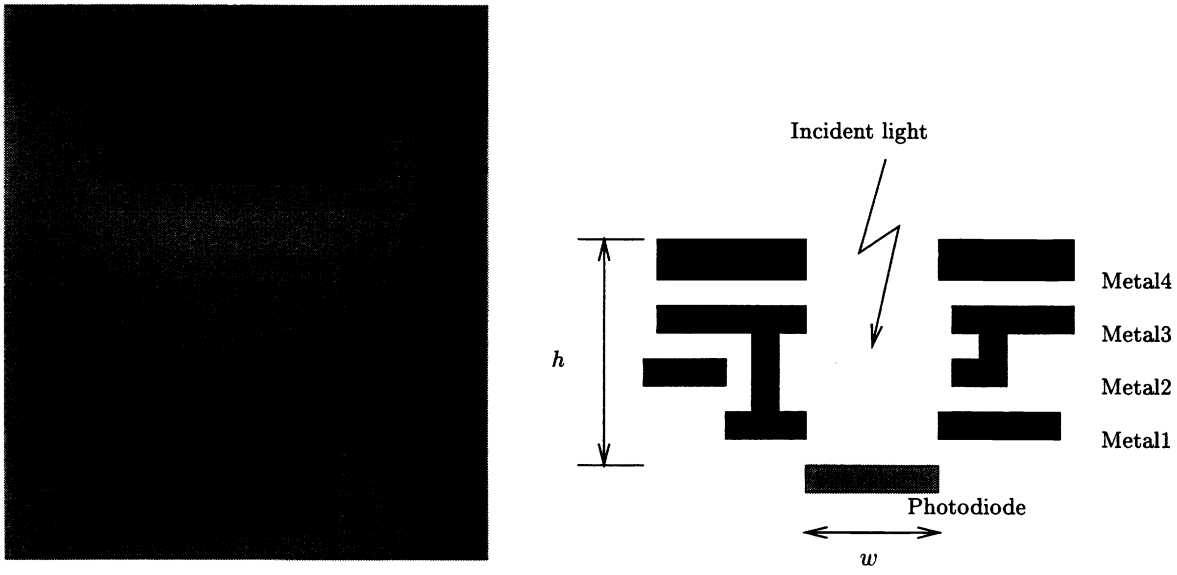

Figure 3. (a) Top-view SEM image of two DPS pixels showing the square opening through the 4th metal layer enabling incident light to reach the photodiode. (b) Cross-section diagram of a DPS pixel with the 4th metal layer acting as a light shield.

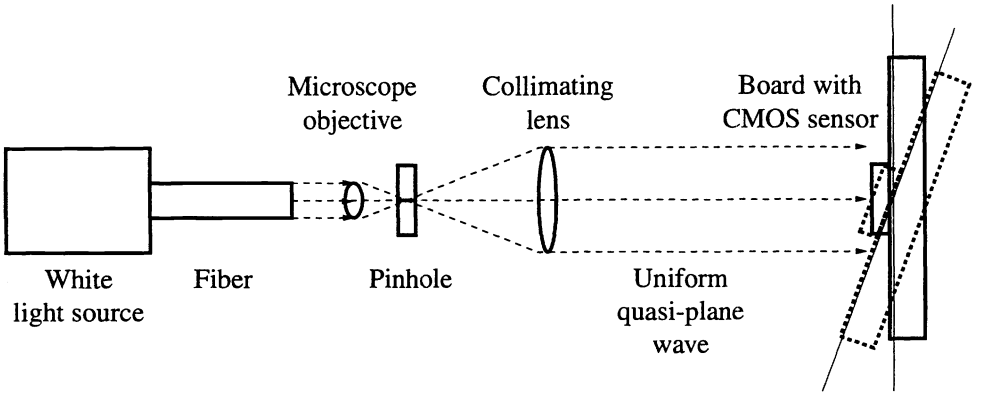

Figure 4. Setup used for the uniform quasi-plane wave experiment.

on an XY-translation stage. The translation stage enables the alignment of the center of the sensor with the rotation axis of the rotation stage. This makes it possible to rotate the sensor, while minimizing translation. The data from the sensor is captured by a digital frame grabber.

Prior to each experiment, we confirm the stability of the white light source by comparing several frames taken at the same illumination and angle. We then fix the illumination level of the source and the integration time for the sensor throughout the experiment. We set the illumination level high enough to minimize integration time, and thus the effect of dark current, while maintaining high SNR. We then position the rotation stage to the desired angle and capture an image of the light field. To reduce non-uniformity, we average the response of the center 30×30 pixels. This is repeated for different angles in both directions. We define the *normalized QE* for a pixel as the ratio of the average pixel response to the peak average pixel response. The peak average response is typically that of an on-axis pixel.

The results are summarized in Figure 5 for each pixel array quadrant. As expected the attenuation increases with angle of incidence. The attenuation can be as high as 35% for a 24° angle (typical full field-of-view (FOV) of a standard SLR camera objective). Note that all graphs exhibit noticeable asymmetry with respect to the direction of the rotation. This is due to the horizontal layout asymmetry inside each pixel block. A surprising result is that the peak response is not always at 0° angle (on-axis). For the 2nd and 4th pixel quadrants the peak occurs at a 12° angle. The reason is again layout asymmetry. *

2.3. Uniformly Illuminated Surface Imaging Experiment

In this experiment, we uniformly illuminate a quasi-Lambertian surface and measure the on and off-axis pixel responses using imaging optics. The purpose of this experiment is to explore the effect of pixel vignetting in a more realistic image capture setting. Note that in this experiment each pixel has a different response based on its location in the array.

The setup used is shown in Figure 6. It consists of a uniformly illuminated quasi-Lambertian surface using a white light source, a $f/1.2$ 16mm imaging lens providing a 24° angle full FOV, and the image sensor.

Again, prior to the experiment, we confirm the stability of the white light source by comparing several images taken at the same illumination level. We set the illumination level high enough to minimize integration time. We then take a set of 10 images and average them to reduce any fluctuations due to temporal noise. The off-axis irradiance attenuation due to the cosine-4th effect of the imaging lens is corrected for prior to analyzing the data. Figure 7 plots the relative mean pixel response for the center row as a function of angle for the chief ray. The response of each pixel array quadrant is presented separately.

*This asymmetry was reported in our earlier work on characterizing FPN for this sensor.[7]

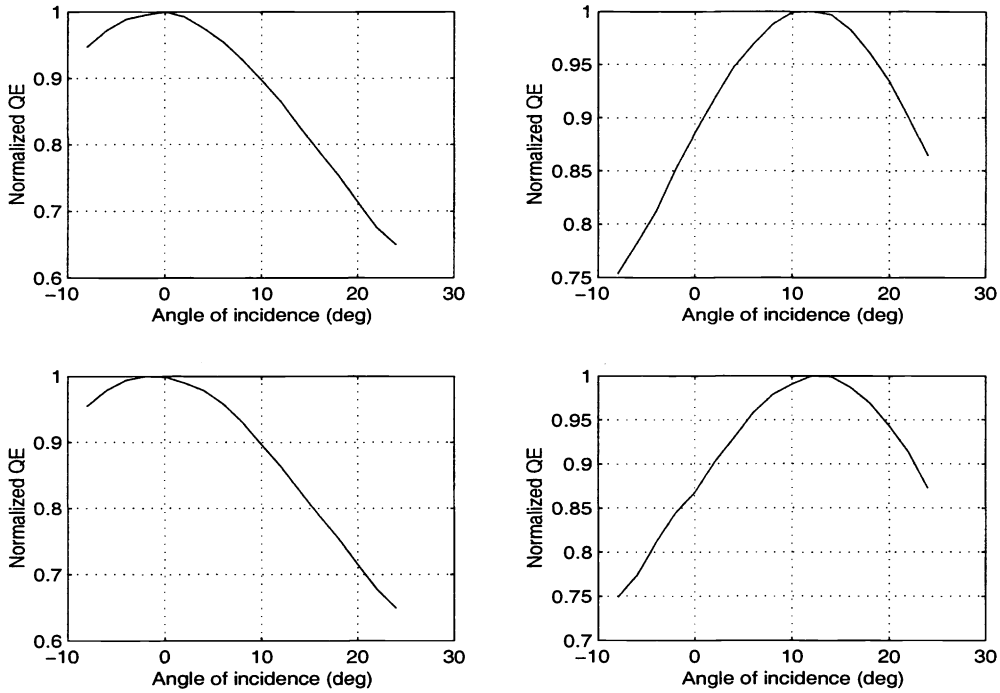

Figure 5. Normalized QE as a function of angle of incidence for each of the 4 pixels in a 2 × 2 DPS pixel block (see Figure 2) during uniform quasi-plane wave illumination.

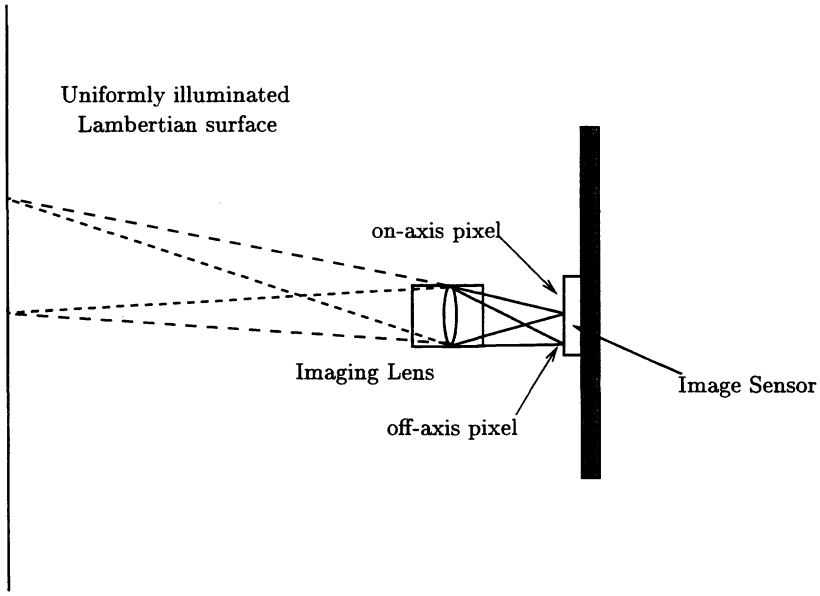

Figure 6. Setup used for uniformly illuminated surface imaging experiment.

The attenuation increases with angle and can be as high as 20% for a 12° angle. This corresponds to half the full FOV of a telephoto lens with twice the focal length of a standard SLR camera objective.

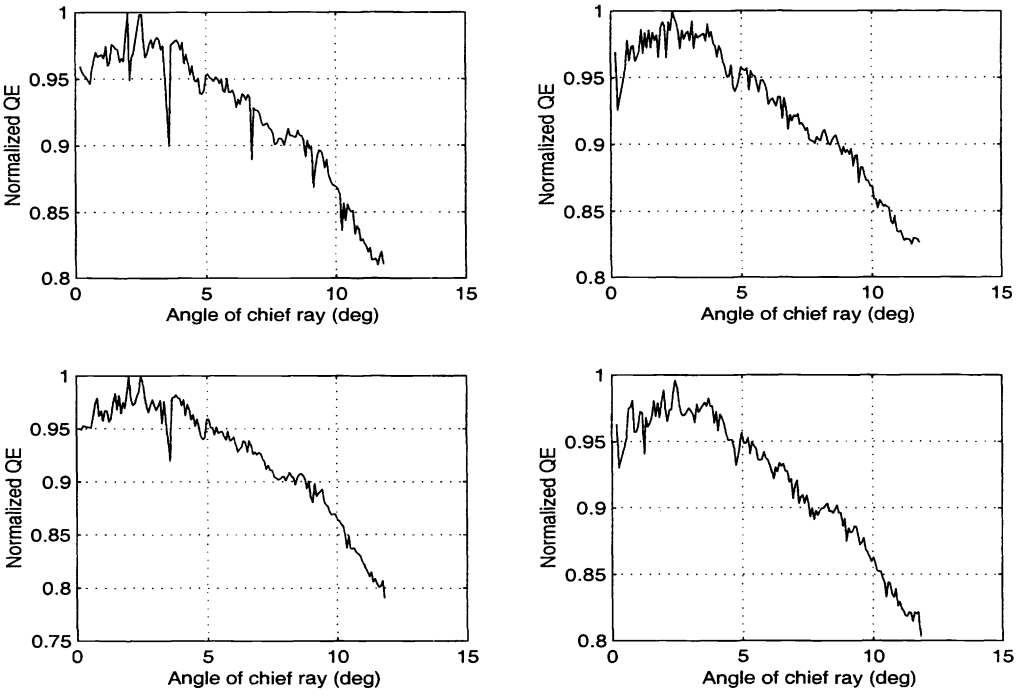

Figure 7. Normalized QE as a function of angle of incidence for each of the 4 pixels in a 2 × 2 DPS pixel block (see Figure 2) while imaging a uniformly illuminated surface.

3. GEOMETRIC MODEL AND ANALYSIS

In the previous section, we experimentally demonstrated the QE reduction of off-axis pixels. In this section, we construct simple geometric models of the pixel and the imaging optics to help support the hypothesis that the observed QE reduction is due to pixel vignetting. These models can also be used in planning the pixel design and layout or in selecting appropriate imaging optics. Of course, more accurate ray-tracing and diffraction beam propagation simulations, *e.g.* Code V,[11] can be used for verification after the layout is completed.

We first analyze the simple case of illumination by a uniform plane wave. We then analyze the case of imaging a uniformly illuminated Lambertian surface through a lens.

3.1. Uniform Plane Wave Illumination Model

Figure 8 shows the cross-section of the tunnel leading to the photodiode. It consists of two layers of dielectric: the passivation layer and the combined silicon dioxide layer. An incident uniform plane wave is partially reflected at each interface between two layers. The remainder of the plane wave is refracted. The passivation layer material is Si_3N_4. It has an index of refraction n_p and a thickness h_p, while the combined oxide layer has an index of refraction n_s and a thickness h_s. If the uniform plane wave is incident at an angle θ, it reaches the photodiode surface at an angle:

$$\theta_s = \sin^{-1}(\frac{\sin\theta}{n_s}).$$

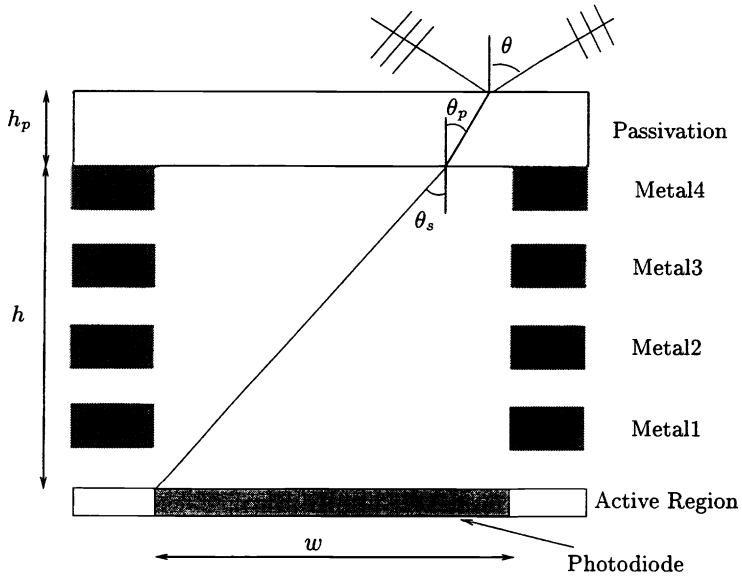

Figure 8. Cross-section of the tunnel of a DPS pixel leading to the photodiode.

Assuming an incident radiant photon flux density E_{in}(photons/s×m^2) † at the surface of the chip, the photon flux density reaching the surface of the photodiode is given by

$$E_s = T_p T_s E_{in},$$

where

$$T_p = \frac{n_p \cos\theta_p}{\cos\theta}\left(\frac{t_{\parallel p}^2}{2} + \frac{t_{\perp p}^2}{2}\right)$$

is the fraction of incident photon flux density transmitted through the passivation layer, where

$$\theta_p = \sin^{-1}\left(\frac{\sin\theta}{n_p}\right)$$

and

$$T_s = \frac{n_s \cos\theta_s}{n_p \cos\theta_s}\left(\frac{t_{\parallel s}^2}{2} + \frac{t_{\perp s}^2}{2}\right)$$

is the fraction of incident photon flux density transmitted through the combined SiO_2 layer. The t terms denote the transmission coefficients for the parallel and perpendicular components of the electromagnetic field of the plane wave. Assuming the same permeability for the three layers, the transmission coefficients are given by

$$\begin{aligned}
t_{\parallel p} &= \frac{2\sin\theta_p \cos\theta}{\sin(\theta+\theta_p)\cos(\theta-\theta_p)} \\
t_{\perp p} &= \frac{2\sin\theta_p \cos\theta}{\sin(\theta+\theta_p)} \\
t_{\parallel s} &= \frac{2\sin\theta_s \cos\theta_p}{\sin(\theta_p+\theta_s)\cos(\theta_p-\theta_s)} \\
t_{\perp s} &= \frac{2\sin\theta_s \cos\theta_p}{\sin(\theta_p+\theta_s)}
\end{aligned}$$

†Since we are using geometric optics here we do not need to specify the spectral distribution of the incident illumination.

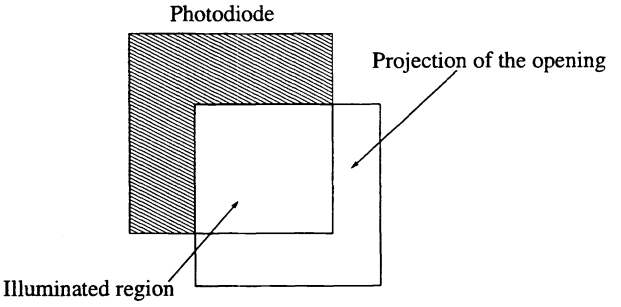

Figure 9. The illuminated region at the photodiode is reduced to the overlap between the photodiode area and the area formed by the projection of the square opening in the 4th metal layer.

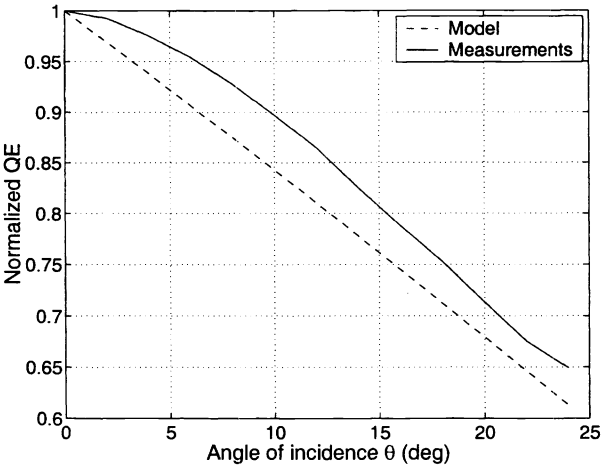

Figure 10. Modeled and measured normalized QE versus angle of incidence θ.

Now, because the plane wave strikes the surface of the photodiode at an oblique angle θ_s, a geometric shadow is created, which reduces the illuminated area of the photodiode as depicted in Figure 9. Taking this reduction into consideration and using the derived E_s we can now calculate the photon flux incident at the photodiode surface:

$$\Phi(\theta) = T_s T_p E_{in}(1 - \frac{h}{w}\tan\theta_s)\cos\theta_s$$

Figure 10 plots the normalized photon flux $\Phi(\theta)/\Phi(0)$, which is the same as normalized QE, as a function of angle of incidence θ and the corresponding experimental results (from Figure 5).

Note that our simple model predicts the QE reduction trend. The discrepancy between the experimental and analysis results can be attributed to the simplicity of our model and the fact that the photon absorption of the photodiode is not uniform over its area.

3.2. Uniformly Illuminated Surface Imaging Model

Here we use the geometric model of the pixel in Figure 8 and a simple geometric model of the imaging lens. The lens is characterized by two parameters: the focal length f and the $f/\#$. To model the setup used in our second experiment, we consider the imaging of a uniformly illuminated Lambertian surface. Figure 11 shows the illuminated area for on and off-axis pixels. Since the incident illumination is no longer a plane wave, it is difficult to analytically solve for the normalized QE as before. Instead, we numerically solve for the incident photon flux assuming the same tunnel geometry and lens parameters as before.

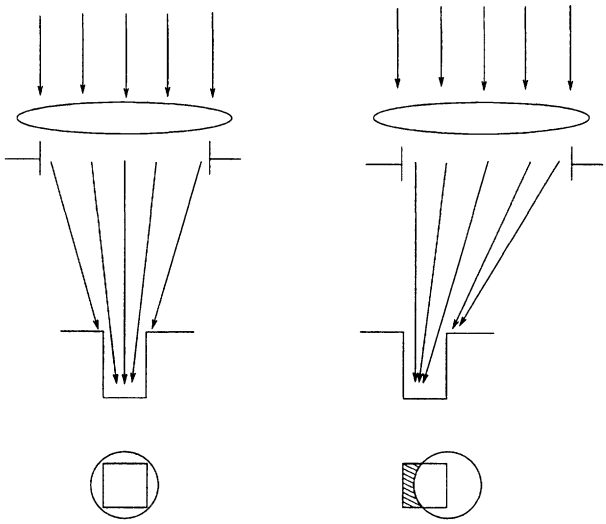

Figure 11. Ray diagram showing the imaging lens and the pixel as used in the uniformly illuminated surface imaging model. The overlap between the illuminated area and the photodiode area is shown for on and off-axis pixels.

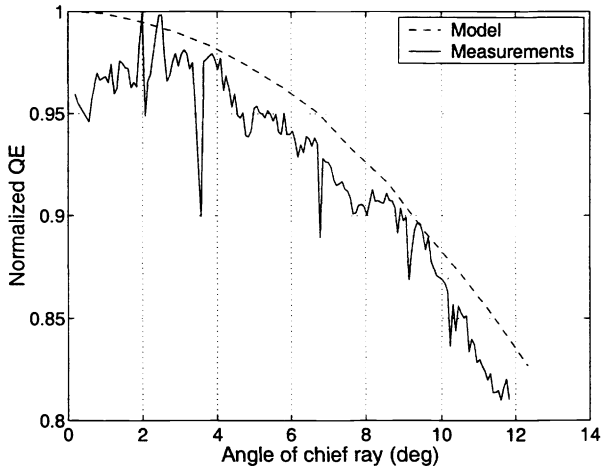

Figure 12. Modeled and measured normalized QE versus angle of incidence θ of the chief ray.

First, we use this model to compare the QE for an on-axis pixel to the case where the photodiode is at the surface of the chip, which can be implemented using thin film , *e.g.* amorphous silicon. We find that the QE is reduced by 40%.

Figure 12 plots the normalized QE versus the angle of the chief ray of the incident light cone. Note that the angle of the chief ray ranges from 0° to half the FOV, which is determined by the focal lens and the sensor array dimensions. Again the simple geometric model predicts the QE reduction trend observed in the experiment.

As CMOS technology scales, we expect the QE reduction due to pixel vignetting to become increasingly severe. This is due to the fact that the interconnect layer thickness does not scale as fast, if at all, with technology as the planar feature sizes. As a result, whether we take advantage of scaling by shrinking the pixel or by adding more transistors and metal layers to it, the ratio of the height of the tunnel leading to

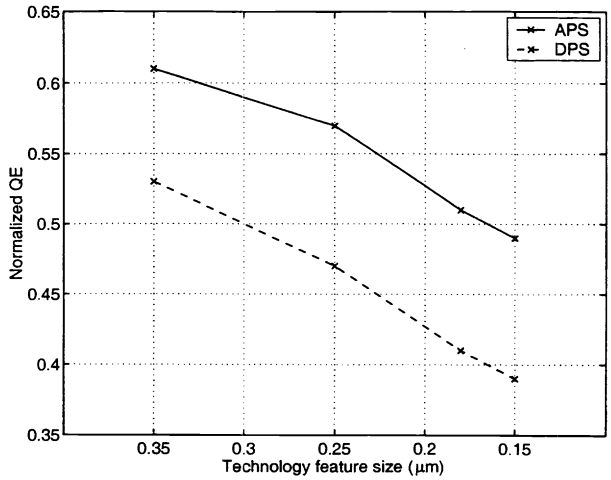

Figure 13. Normalized QE at a 24° angle as technology scales for a standard photodiode APS pixel and for a photodiode DPS pixel.

the photodiode h to the pixel dimension w increases with scaling. The experimental and analysis results demonstrate that using more metal layers in the pixel will result in significant QE reduction. Pixel vignetting results in similar QE reduction even if we only shrink pixel size. To demonstrate this, we plot in Figure 13 the relative QE reduction at a 24° angle for a standard photodiode APS[5] pixel using only two layers of metal as a function of technology generation assuming a constant 30% fill factor. For comparison, we also plot the QE reduction for a DPS pixel using the multiplexed pixel level ADC , which uses 4 layers of metal, with the same fill factor.

4. CONCLUSION

We presented experimental results showing significant reduction of QE for off-axis relative to on-axis pixels. We hypothesized that the reduction is due to *pixel vignetting*. To help support this hypothesis we used simple geometric models for the pixel and imaging optics to compare the QE of on and off-axis pixels. We found the analysis to predict similar QE reduction to the experimental results. As technology scales and the h/w increases, we showed that QE reduction due to pixel vignetting becomes more severe even for a 2-layer metal APS pixel.

There are several potential solutions to the pixel vignetting problem. We provide only a brief discussion of these solutions here:

- **Tapered tunnel**: It is possible to layout the interconnect layers around the photodiode so that the tunnel tapers toward the photodiode to reduce pixel vignetting. This, however, is likely to reduce fill factor (for a fixed pixel size). One would need to investigate the trade-off between reducing fill factor and improving pixel vignetting to assess the net effect of a tapered tunnel.
- **Telecentric imaging lens**: Specially designed imaging optics, such as telecentric lens systems, can reduce pixel vignetting by keeping the chief ray of the incident light cone for off-axis pixels nearly the same as for on-axis pixels. However, these systems have their own complexities and drawbacks.[10]
- **Microlenses**: QE can be increased using microlenses.[8,9] The design and manufacturing of these microlenses must, however, take into consideration the geometry of the tunnel. The improvement in on-axis QE can be considerable. For off-axis pixels, it is not clear how much improvement, if any, is achieved without the use of a telecentric imaging lens or an unconventional angle-dependent microlens design, which may not be practical. Another important consideration is the material needed. To

focus the light onto the photodiode surface, the focal length of the microlens may be too long to be manufactured using silicon dioxide. In this case, other materials such as polymethyl methacrylate (PMMA)[12] may be used, which increases the cost of the microlens fabrication.

- **Thin film photodiode**: As discussed in subsection 3.2, QE can be substantially improved even for on-axis pixels by moving the photodiode to the surface of the chip. This can be implemented using thin film technology, *e.g.* amorphous silicon. This approach may, however, suffer from other problems: manufacturing cost, lag, *etc.*

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