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Monolithic Integration of Electronics and Sub-wavelength Metal Optics in Deep Submicron CMOS Technology

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ABSTRACT

The structures that can be implemented and the materials that are used in complementary metal-oxide semiconductor (CMOS) integrated circuit (IC) technology are optimized for electronic performance. However, they are also suitable for manipulating and detecting optical signals. In this paper, we show that while CMOS scaling trends are motivated by improved electronic performance, they are also creating new opportunities for controlling and detecting optical signals at the nanometer scale. For example, in 90-nm CMOS technology the minimum feature size of metal interconnects reaches below 100 nm. This enables the design of nano-slits and nano-apertures that allow control of optical signals at sub-wavelength dimensions. The ability to engineer materials at the nanoscale even holds the promise of creating meta-materials with optical properties, which are unlike those found in the world around us. As an early example of the monolithic integration of electronics and sub-wavelength metal optics, we focus on integrated color pixels (ICPs), a novel color architecture for CMOS image sensors. Following the trend of increased integration in the field of CMOS image sensors, we recently integrated color-filtering capabilities inside image sensor pixels. Specifically, we demonstrated wavelength selectivity of sub-wavelength patterned metal layers in a 180-nm CMOS technology. To fulfill the promise of monolithic photonic integration and to design useful nanophotonic components, such as those employed in ICPs, we argue that analytical models capturing the underlying physical mechanisms of light-matter interaction are of utmost importance.

INTRODUCTION

Device dimensions in 21st-century complementary metal oxide semiconductor (CMOS) technology are reaching well into the nanometer regime [1]. While scaling enables increased clock speeds for central processing units (CPUs) and chip densities for random access memories (RAM), it also opens up opportunities for photonic device fabrication. In fact, integrated optics and photonics devices are already being implemented using processing techniques that are directly leveraged from semiconductor technology [2]. In this section, we briefly introduce CMOS technology and we evaluate some of its characteristics and its suitability from a photonics point of view.

CMOS technology is a complete process flow sequence, in which several technologies are combined to produce very large scale integrated (VLSI) circuit chips. Two important technologies in this flow are the front-end and the back-end technology.

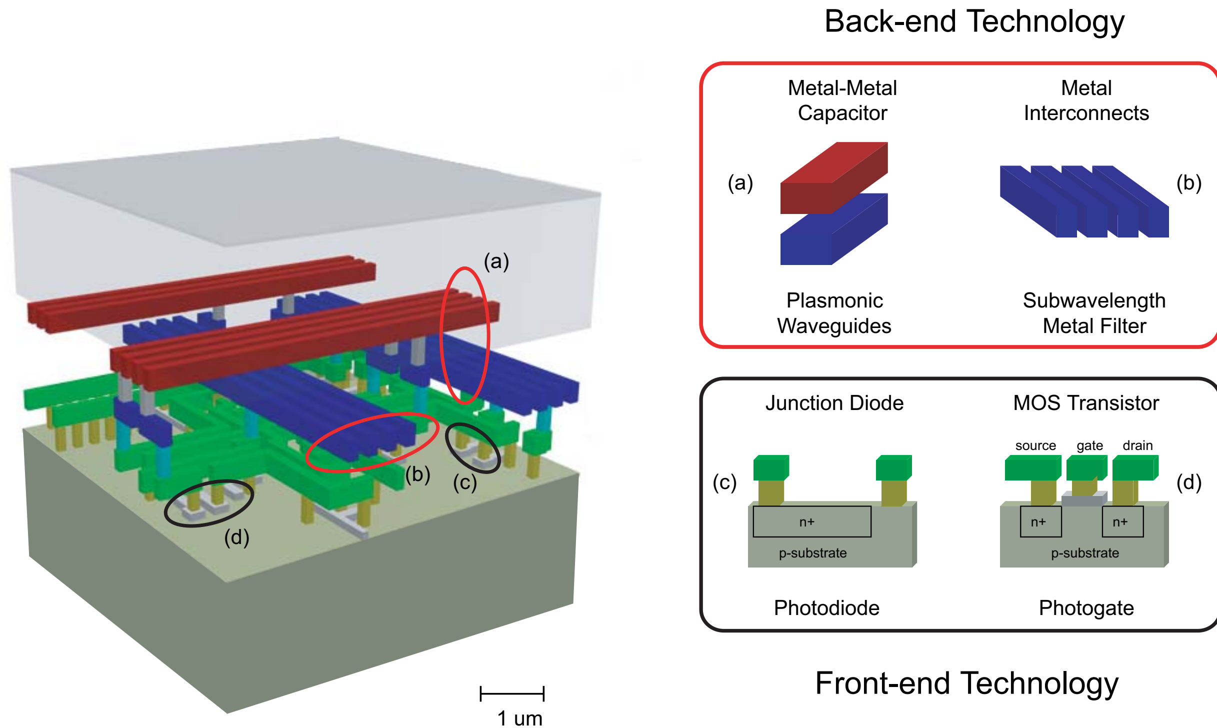


Figure 1. Three-dimensional rendering of a 10 micron by 10 micron area of a VLSI chip implemented in CMOS technology. Shown is the silicon substrate (grayish-green surface at the bottom). Front-end technology defines the active devices, e.g., diodes (c) and transistors (d). The back-end technology defines capacitors (a) and interconnects (b). It consists of metal-1 (green rectangles), metal-2 (blue rectangles), and metal-3 wires (red rectangles) separated by dielectric layers (transparent) and connected by vias.

Front-end technology comprises a series of processing steps required to define active regions, N and P wells, gates, and sources/drains in the silicon (Si) substrate [3]. These steps are crucial for the creation of active devices (e.g., transistors or junction diodes), but are only introduced here for completeness. Here, we focus on the back-end technology, i.e., interconnect layers, contacts, vias, and dielectric layers that wire the active devices into circuits and systems.

While CMOS technology is a planar process, this does not imply that chips are two-dimensional. Figure 1 depicts a three-dimensional rendering of a 10 micron by 10 micron area of a VLSI chip. The insets identify some of the important structures that are created using back-end technology (e.g., metal-metal capacitors or metal interconnect wires). The back-end technology is responsible for creating most of the structures visible in this picture and typically stretches for about 10 micron above the Si substrate (grayish-green surface at the bottom). Low-resistance metal interconnects (green, red, and blue rectangles) wire the different parts of the chip and provide clock distribution. They are structured as a series of closely spaced parallel wires (red and blue rectangles). The interconnect layers are separated in the vertical dimension by high-resistivity dielectric layers. Vias (gray vertical stubs) connect two levels of interconnects. This completes the picture that a CMOS technologist has of the back-end technology.

However, one might pose the question: "What would a photonics researcher see when looking at the same picture?" Given the absorption properties of Si, the substrate is suitable for the detection of visible optical radiation. This can be achieved through the realization of photogates or photodiodes in front-end technology. These devices are nearly identical in implementation than the active devices used for electronic purposes (MOS transistors and junction diodes). In fact, photodetectors are currently being used as the photosensitive sites in the pixels of mass-produced charge-coupled device (CCD) and CMOS image sensors. In this paper, however, we focus on the optical properties associated with metallic structures that can be built in back-end technology. From a photonics point of view, an interconnect bus looks like a metal wire grid. The use of wire grids for filtering electromagnetic radiation goes back to the early experiments of Heinrich Hertz in the late 1800s [4]. In the field of microwave engineering, regular metal grids have been used for a long time as filters, transmitting some wavelengths and blocking others [5]. In fact, as a result of continued advances in the manufacturing technology of electronic ICs, metal grids with periodicity commensurate with the wavelength of near-infrared light have been demonstrated [6].

Over the past 25 years, the minimum lithographic feature size in CMOS technology has decreased by thirty percent every three years and has resulted roughly in a doubling of the number of transistors per chip every two years [1]. This trend is usually referred to as Moore's law [7]. Figure 2 shows the minimum half-pitch for a series of parallel wires implemented using the metal-1 layer in a CMOS logic process as a function of time [1]. While scaling is clearly being achieved to improve electronic performance of VLSI circuits, it also creates new ways to control light. With the minimum metal feature sizes available in 90-nm CMOS technology, sub-wavelength periodicities can now be achieved for the optical regime. This means that an interconnect bus or wire grid, for example, can be used as an optical filter to selectively change the transmission of visible electromagnetic radiation.

As device size decreases and chip density increases, interconnects have become a critical aspect of chip performance. Circuit time delays associated with interconnects have not kept pace with increasing device speeds. The resistance-capacitance (RC) time delay of a signal propagating along a metal interconnect (Fig. 3) is to first order obtained by treating it as a distributed, unterminated transmission line and is given by [3]

$$\tau_{\text{interconnect}} = 0.89\, RC\,, \tag{1}$$

where R is the line resistance and C is the total capacitance associated with the line. With scaling, interconnect width and separation follow the minimum feature size $F_{\min}$. This means

$$\tau_{\text{interconnect}} \propto \frac{\varepsilon_{\text{dielec}}}{\sigma_{\text{metal}}} \frac{L^2}{F_{\min}^2}\,, \tag{2}$$

where L is the interconnect length, while $\varepsilon_{\text{dielec}}$ and σ_{metal} represent the permittivity (or dielectric constant) of the dielectric surround and conductivity of the interconnect metal.

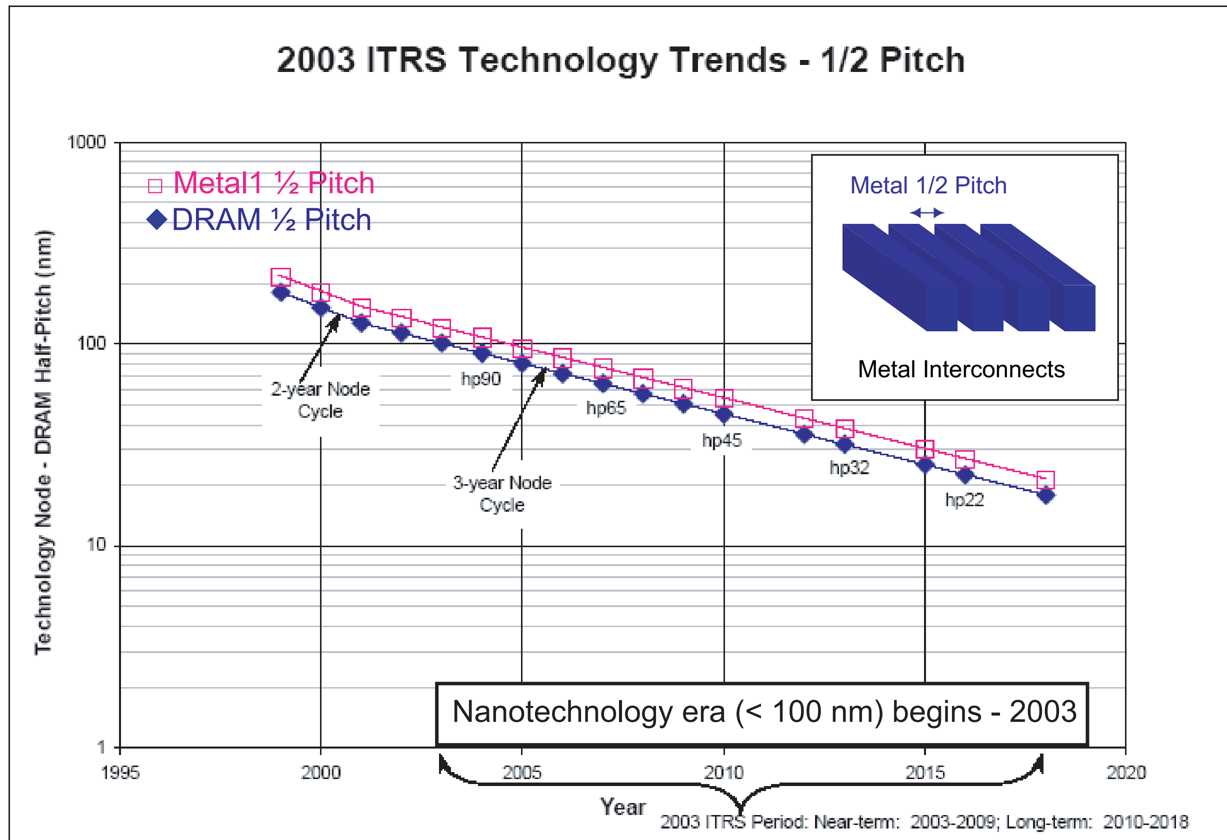


Figure 2. Scaling of the minimum pitch for metal interconnects implemented in a CMOS logic process. The figure shows the trend for both DRAM and metal-1 half-pitch according to the International Technology Roadmap for Semiconductors (ITRS) [1].

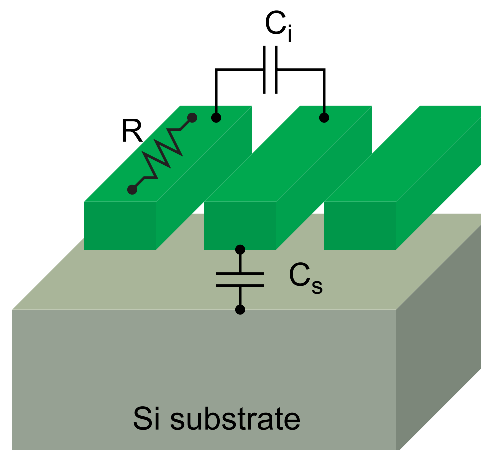


Figure 3. Interconnect structure for RC analysis. The green rectangles on top are the metal interconnects surrounded by SiO_2. At the bottom is the Si substrate (grayish-green). R is the line resistance, while C_i and C_s are the line-to-line and line-to-substrate capacitance, respectively. The total capacitance follows as $C = C_i + C_s$.

Global interconnect lengths usually increase as technology scales and thus RC delays tend to increase for a given interconnect material system. In order to maintain the distribution of clock and various other signals to different parts of a VLSI chip, however, RC delay time needs to keep pace with the decreasing gate delay time. This can be achieved by a careful choice of the materials.

The material system, on which back-end technology has traditionally relied, consists of aluminum (Al) for the metallic layers and silicon dioxide (SiO_2) for the dielectric layers. Aluminum features relatively high conductivity ($\sigma_{Al} = 3.64\times10^{7}\ S/m$), adheres well to SiO_2 and Si (due to the formation of its native oxide), and makes good electrical contact to heavily doped Si. SiO_2 has a relatively low static dielectric constant ($\varepsilon_{SiO_2} = 4.1$) and yields very controllable, stable and reproducible dielectric layers that serve to separate the metallic layers [3].

To reduce RC time delay in the face of scaling issues, one can increase conductivity and decrease permittivity. Three materials have higher conductivity than Al: silver, copper (Cu), and gold. Silver has corrosion problems and poor electromigration resistance, while gold has marginally higher conductivity than Al and suffers from device contamination issues. Cu has an almost-twice higher conductivity ($\sigma_{Cu} = 5.88\times10^{7}\ S/m$) than Al and has better electromigration properties. Hence, Cu has been chosen as a replacement for Al, even though this meant the introduction of a damascene process [3]. The dielectric constant ($\varepsilon_{\text{dielec}}$) of the interlayer dielectrics also affects device performance. To fulfill the requirements for VLSI, low dielectric constant (low-k) materials have been recently developed, e.g., hybrid organic-siloxane polymer (HOSP) with $\varepsilon_{HOSP} = 2.5$ [8] or Nanoglass with $\varepsilon_{\text{Nanoglass}} = 2.1$ [9]. This also results in a two-fold performance improvement.

While the back-end technology materials are chosen for their electronic properties, they are also suitable for doing photonics. For example, low-k dielectrics also have lower dielectric constants in the optical regime [8,9]. Since the wavelength of light λ is reduced inside the dielectrics ($\lambda = \lambda_0 / \sqrt{\varepsilon_{\text{dielec}}}$, where λ_0 is the wavelength in vacuum) that surround the metallic structures, a wire grid can only act as a zeroth-order diffraction grating when its period is smaller than λ. Therefore, reducing $\varepsilon_{\text{dielec}}$ in the optical regime helps with scaling. Equally important are the losses introduced in the metal through Joule heating. It turns out that Cu not only has a larger static conductivity than Al, but also features lower losses in the optical regime [10,11].

In summary, the structures that are implemented in CMOS back-end technology feature both electronic and photonic functionality. The decrease in feature size, which is driven by an increase in electronic performance, also benefits photonic performance. Finally, the materials used in CMOS technology are chosen for their electronic characteristics, yet they also exhibit suitable photonic properties. These observations are the motivation for using of CMOS back-end technology as a platform for research in nanophotonics and light-matter interaction at the nanoscale with the potential for monolithic integration of both electronics and photonics.

MONOLITHIC INTEGRATION OF ELECTRONICS AND PHOTONICS

Electronic ICs have transformed the world we live in. They have propelled us into the information age and will continue to do so as CMOS technology keeps scaling. Current information technology also often uses light (photons) to transmit, store, and display information. Photonic technology is thus equally intimately interwoven with information technology and will continue to be so into the foreseeable future. It is therefore expected that monolithic integration of photonic and electronic ICs will not only advance information processing, but also will offer unique opportunities for future interconnects, telecommunication and biosensing devices.

To achieve monolithic integration, a major challenge needs to be overcome: in contrast to electrons, which have a very small footprint (<< 1 nm), visible and infra-red photons have sizable dimensions (100s nm). This inherent size mismatch aggravates the integration of electronic and photonic ICs. Recent advances in nanophotonics, i.e., the manipulation of light at a length scale smaller than its wavelength, place us in a unique position to start addressing this challenge. Nanophotonics includes both photonic crystals [12] and plasmonic devices [13]. Both approaches are central to molding the flow of light below the diffraction limit and, hence, to miniaturizing photonic ICs. It is therefore timely to explore the integration of photonic functionality with deep submicron CMOS technology.

In this section, we describe an early example of monolithic integration of electronics and sub-wavelength metal optics in deep submicron CMOS technology. We present experimental work from the field of CMOS image sensors [14], involving integrated color pixels, a novel color architecture for CMOS image sensors.

An important trend in digital camera design is the development of CMOS image sensors. These sensors are being scaled with CMOS technology to enable an increasing level of integration of capture and processing to reduce system power and cost [15]. Toward completing design integration of color image sensors in CMOS technology, we have explored the possibility of introducing wavelength selectivity with only standard processing steps, i.e., without inserting the traditional color filter array (CFA, Fig. 4a). Specifically, we have implemented filters that consist of sub-wavelength patterned metal layers placed within each pixel to control the transmission of light through the pixel to its photodetector. We refer to such pixel design as an integrated color pixel (ICP, Fig. 4b). ICPs may be useful for digital camera applications but may be even more suited to multispectral imaging and a variety of other image-sensing applications.

Monolithic integration of the optical filters inside image sensor pixels offers several potential advances. Placing the filters close to the photodetector reduces color cross talk, and pixel vignetting and increases the efficiency of microlenses. Controlling wavelength responsivity in the pixel design process eliminates the need for additional CFA manufacturing steps [14]. Why have wire grids not been used for color filtering in the visible light regime? To control light in the visible wavelength range with wire grids requires periodicities smaller than the visible wavelengths. This has been impossible until recent 180-nm CMOS technology and even with the wire sizes possible here, we are on the edge of controlling visible wavelengths.

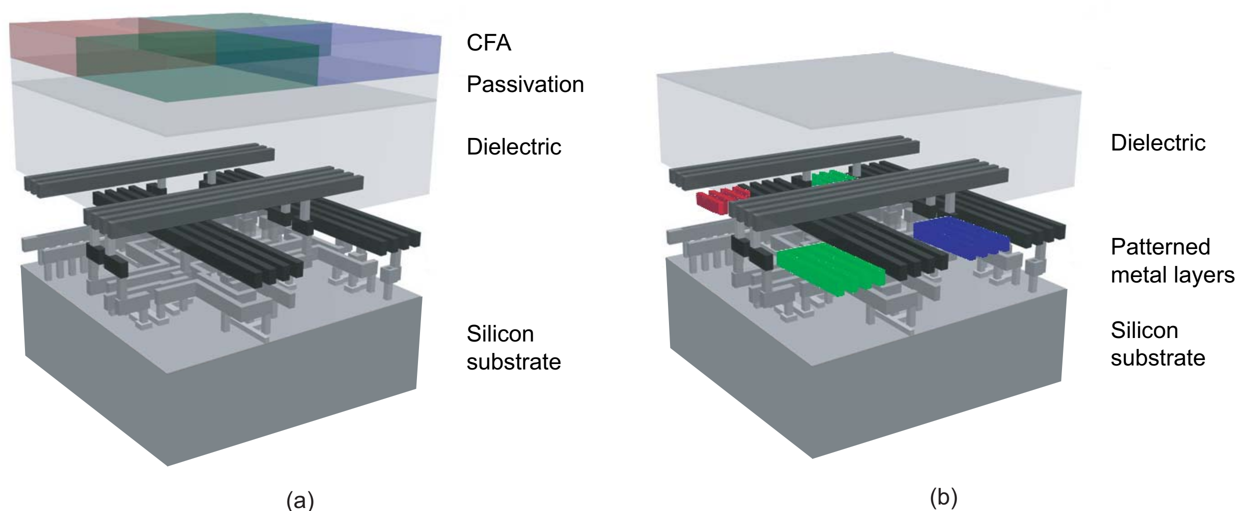


Figure 4. Geometry of four pixels in a CMOS color image sensor. (a) A conventional arrangement including a red-green-blue (RGB) color-filter array placed on the sensor surface. (b) The integrated color pixel arrangement that contains patterned metal layers (shown in color) within the pixel tunnels.

To investigate the use of sub-wavelength patterned metal layers as filters for color imaging, we implemented ICP test structures in a standard 180-nm CMOS technology. Periodic patterns were created in the metal layers already present in the process. These patterns comprised an array of elements whose gap widths were restricted by the process design rules and ranged from 270 to 540 nm. The refractive index of the surrounding dielectric (SiO_2) is 1.46. In air the visible wavelength regime is roughly 400-750 nm; in this medium the effective visible wavelength regime is roughly 270-510 nm. We implemented ICPs using a standard three-transistor active-pixel-sensor (APS) circuit. A photomicrograph of the chip with the ICP test structures is shown in Fig. 5a. The test structures (Fig. 5b) included one-dimensional (1D) and two-dimensional (2D) patterns with a periodicity (metal width + gap width) ranging from 540 to 810 nm and a gap width ranging from 270 to 540 nm.

The spectral transmittance through the patterned metal layers is measured indirectly by comparing the spectral responsivity of the ICP with that of an uncovered reference pixel. Figure 6 shows the spectral transmittance of a 1D patterned metal layer consisting of 270-nm-wide wires and gap widths ranging from 270 to 540 nm, where sizes represent the design specifications. Transmittance is shown for collimated illumination polarized with the electric field parallel to the wires (TE; Fig. 6a) and with the electric field perpendicular to the wires (TM; Fig. 6b). For TE polarization (Fig. 6a), for example, there is a constant but attenuated transmission region (left) and a cutoff region (right). The location of the cutoff region is determined by the gap width and the cutoff wavelength increases with increasing gap width. The TM transmittances in Fig. 6b differ in a few ways from the TE transmittances. Mainly, the TM transmittance measurements do decline at longer wavelengths with a steeper falloff which depends on the periodicity rather than gap width.

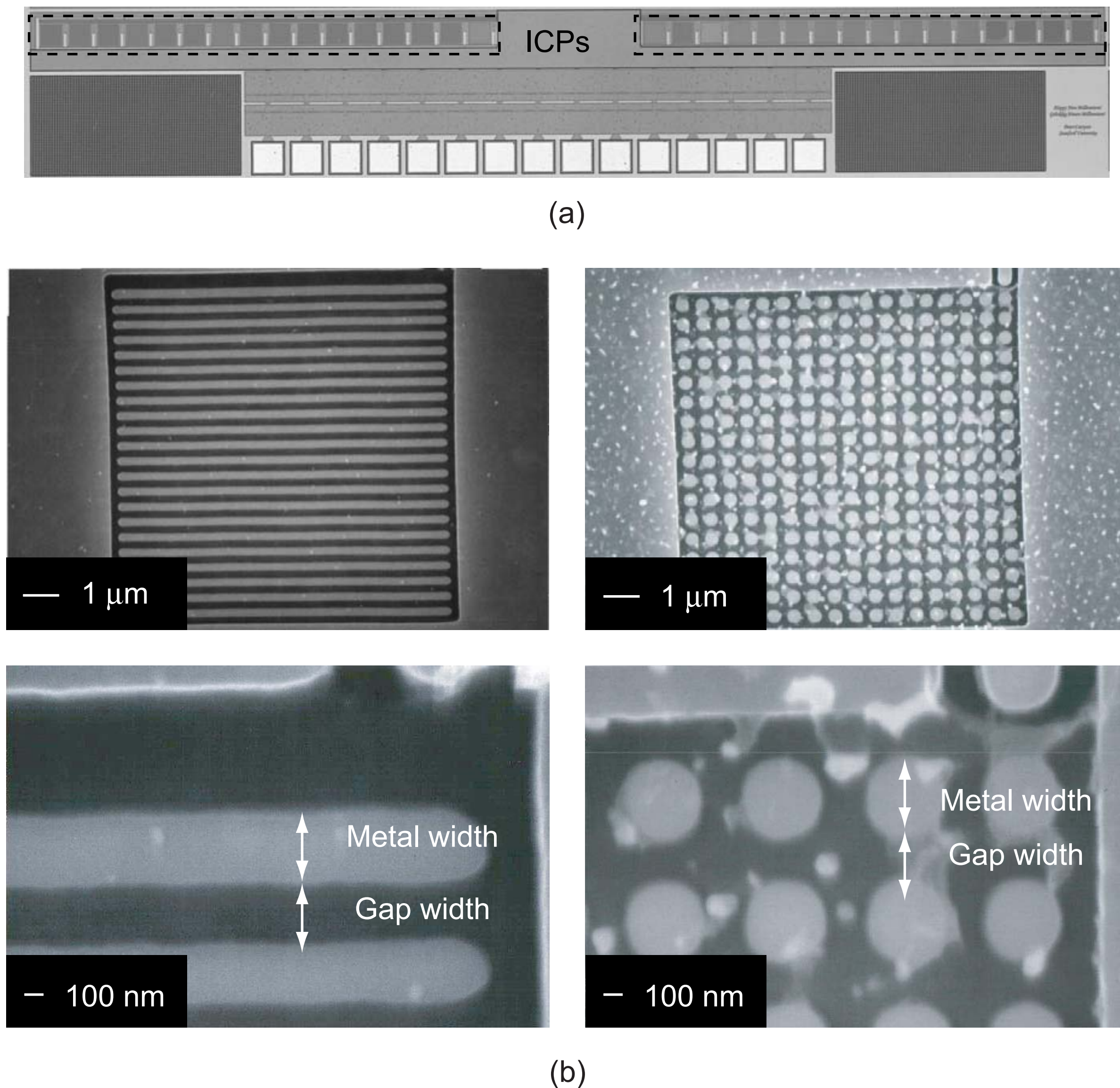


Figure 5. ICP implementation in 180-nm CMOS technology. (a) A photomicrograph of the ICP test structure chip. (b) Scanning electron micrographs of the ICP patterned metal layers. The 1D (left) and 2D (right) patterns are shown at two different spatial resolutions. The white spots, seen particularly on the right, are traces of material that was not removed completely during the deprocessing necessary to make these images.

Measured ICP transmittances are such that a linear combination, e.g., with a 3-by-3 matrix, suffices to produce red, green, and blue color channels with distinct peak sensitivities at approximately 750, 575, and 450 nm, respectively [16,17]. Although first-generation ICPs have a peak transmittance of only 40%, CMOS image sensors in 130-nm CMOS technology will permit smaller features and more flexibility in designing suitable patterns. This is expected to result in ICP transmittance comparable to that of CFAs.

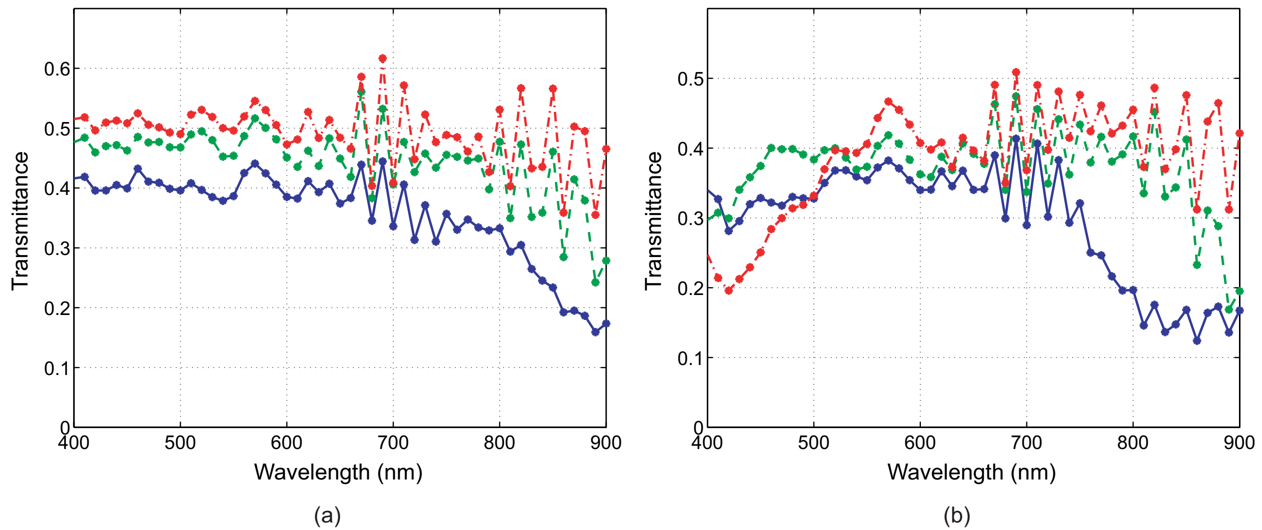


Figure 6. Measured transmittance of 1D ICPs with gap widths designed to be 270 (blue solid curve), 360 (green dashed curve), and 450 (red dash-dotted curve) nm. Wire width is held constant at 270 nm. Measurements are for collimated, polarized illumination: (a) E-field parallel with wires (TE) and (b) E-field perpendicular to wires (TM).

The measured TE and TM transmittance can also be predicted by using a numerical electromagnetic field simulation based on the finite-difference time-domain (FDTD) method [14]. FDTD is a first-principles method and is very valuable in analyzing existing structures. However, the method is slow and requires large amounts of memory, especially for 3D simulations. Moreover, the numerical aspect of the method does not provide the direct physical insight. This is very important when tackling an inverse problem such as filter design, i.e., determining the parameters of a structure so that it would generate the required spectral transmittance. To fulfill the promise of ICPs for color and multispectral imaging the design of patterned metal layers needs to be optimized and analytical models that capture the physical transmission mechanism are essential in guiding the design.

We have shown that a one-mode model [18], in which the sub-wavelength gaps of a 1D patterned metal layer are described in terms of single-mode waveguides, is in fact sufficient to capture the salient features of the ICP wavelength selectivity, even when the metal layer is modeled as a perfect electric conductor (PEC). The model provides closed-form Airy-like formulas for the transmittance of the patterned metal layers and gives physical insight into the transmission mechanism. Given the agreement with measurements, this analytical model should prove useful in optimizing the design of ICPs in CMOS image sensors and can also be straightforwardly extended to 2D patterns for polarization-independent color filtering.

Since feature sizes in 180-nm CMOS technology are not small enough to enable the implementation of the filters featuring the transmittance spectra shown in Fig. 7, we have developed an electron-beam lithography process. In this process, a combination of standard CMOS technology processing steps are combined with additional steps aimed at patterning a topical Al film (Fig. 8).

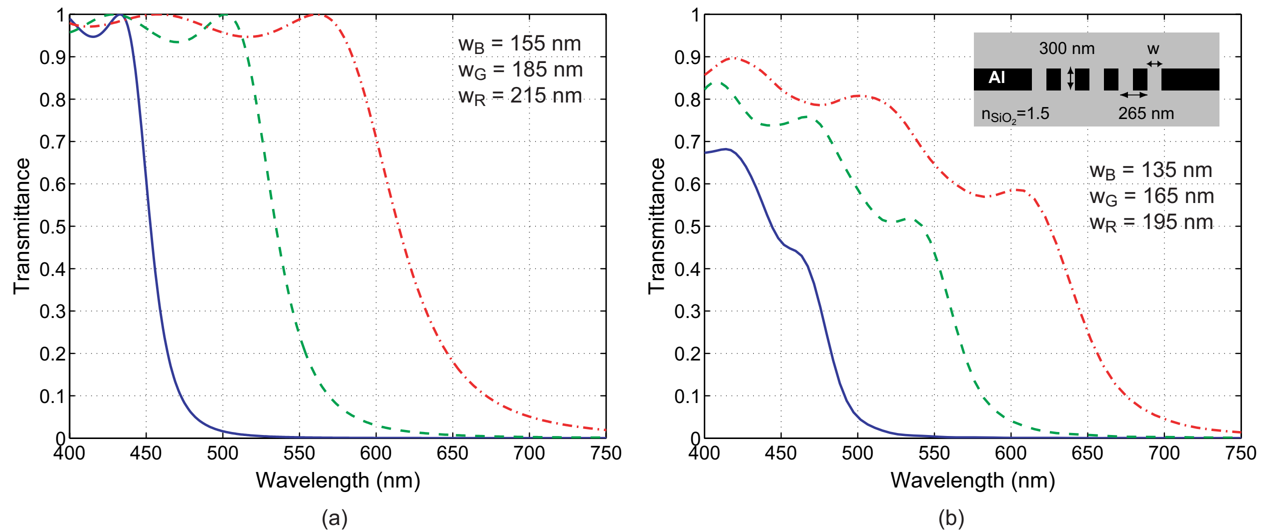
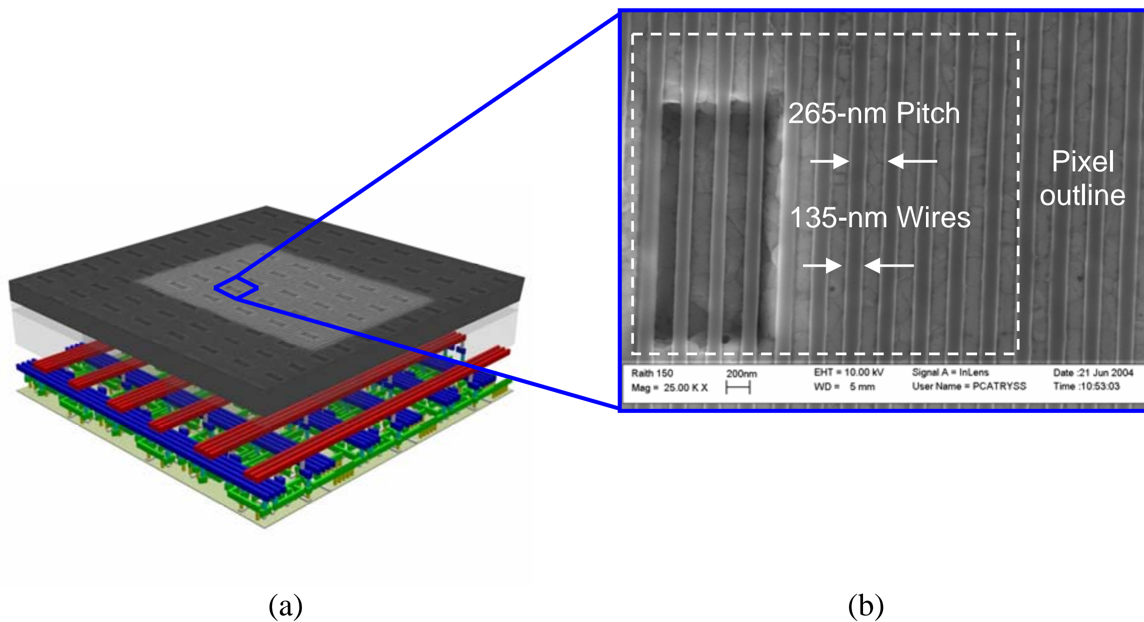


Figure 7. Transmittance of 1D sub-wavelength patterned metal layers suitable for RGB color filters in an ICP. The periodicity of the patterns (Λ) is chosen to assure sub-wavelength behavior for all wavelengths above 400 nm ($\Lambda = 265\,nm < 400\,nm / n_{SiO_2}$). (a) Transmittances obtained using the one-mode model in combination with a PEC assumption for the Al layer ($\lambda_{R,G,B} = 2 n_{SiO_2} w_{R,G,B}$). (b) Transmittance obtained using 2D FDTD simulations with a Drude model for the Al layer. (R: red dash-dotted curve, G: green dashed curve, B: blue solid curve)



(a) (b)

Figure 8. Electron-beam lithography process for sub-wavelength patterning of metal layers. (a) A topical Al layer is deposited on top of a processed 6-inch wafer with fully-functional monochrome CMOS image sensors. (b) Scanning electron micrograph of the sub-wavelength patterned photoresist used as a mask for the etching of the Al layer. Dimensions are for the blue filter with transmittance shown in Fig. 7.

Here, the Al film is applied at the surface as opposed to being embedded in the back-end technology. Yet, the electron-beam lithography process will enable us to define the sub-wavelength features required to prototype and evaluate the performance of the novel ICP color filters using existing 250-nm CMOS image sensor technology. This work is still in progress.

DISCUSSION

We explored the monolithic integration of photonic functionality with CMOS technology at the sub-wavelength scale. The structures that can be implemented and the materials that are used in CMOS IC technology are typically optimized for electronic performance. Upon closer examination, they are also suitable for manipulating and detecting optical signals. We showed that while CMOS scaling trends are motivated by improved electronic performance, they are also creating new opportunities for controlling and detecting optical signals at the nanometer scale. For example, in 90-nm CMOS technology the minimum feature size of metal interconnects reaches below 100 nm. This enables the design of nano-slits and nano-apertures that allow control of optical signals at sub-wavelength dimensions. The ability to engineer materials at the nanoscale even holds the promise of creating meta-materials with optical properties, which are unlike those found in the world around us. As an early example of the monolithic integration of electronics and sub-wavelength metal optics, we focused on integrated color pixels (ICPs), a novel color architecture for CMOS image sensors. Following the trend of increased integration in the field of CMOS image sensors, we recently integrated color-filtering capabilities inside image sensor pixels. Specifically, we demonstrated wavelength selectivity of sub-wavelength patterned metal layers in a 180-nm CMOS technology. To fulfill the promise of monolithic photonic integration and to design useful nanophotonic components, such as those employed in ICPs, we argued that analytical models capturing the underlying physical mechanisms of light-matter interaction are of utmost importance.

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