A 96-Channel Full Data Rate Direct Neural Interface in 0.13μm CMOS

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Abstract

A power and area efficient sensor interface consumes 6.5 mW from 1.2 V supplies while occupying 5 mm x 5 mm in 0.13 μm CMOS. The interface enables full bandwidth access to 96 channels of data acquired from cortical microelectrodes as part of a head-mounted wireless recording system for unconstrained primate neuroscience experiments. Open loop amplification and switched-capacitor (SC) filtering with 2.2 μVrms input referred noise conditions the signals before conversion by 10-bit SAR ADCs with 60.3 dB SNDR and 41.5 fJ/conv step.

Introduction

Acquisition of extracellular neural action potentials (ENAP) and local field potentials (LFP) from cortical brain regions is an important application of low-power mixed-signal IC systems, enabling basic neuroscience research as well as emerging clinical technologies. Research tools created by IC designers are used by scientists in exploring the function of the central and peripheral nervous systems [1-4], and make an impact in the way we diagnose, treat, and understand a broad range of neurological ailments such as epilepsy, chronic pain, obsessive compulsive disorder, and chronic neurodegenerative diseases. We present a 96 channel sensor interface IC that forms the cornerstone of the HermesE [1, 2] next generation wireless neural recording system that enables high channel count recordings from freely-behaving primates. The interface incorporates a novel front end for recording ENAP and LFP that achieves low noise (2.2 μVrms input referred) and high integration density (96 channels on a 5 mm x 5 mm die) while exhibiting power efficiency that is among the best reported. The interface is the first demonstration of a fully SC-conditioned signal path integrated in a massively-multichannel neural interface operating with low voltage (1.2 V) supplies and I/O, and enables a robust and low power head-mounted recording platform.

System Architecture

The system described (Fig. 1) interfaces silicon MEMS electrodes to digital systems, for use in ongoing experimental neuroscience studies of motor behavior and research toward neuroprosthetic systems [1-2, 6]. ENAP signals are amplified and band limited to 0.3-10 kHz with a fully differential front end employing open loop amplification and area-efficient SC band-pass filtering achieving an overall measured noise efficiency factor (NEF) [5] of 5.0 at 2.2 μVrms input referred noise (measured to 100 kHz) using only 0.05 mm² per channel. ENAP/LFP signals are conditioned simultaneously on 4 channels with 3 μVrms and 14 μVrms input referred noise in the ENAP (>100 Hz) and LFP (1-100 Hz) bands respectively. Each channel is digitized at 31.25 kS/s by 10-bit charge redistribution SAR ADCs with 60.3 dB measured SNDR and 41.5 fJ/conv step, and the resulting 30 Mbps raw data stream is transmitted off-chip serially. Scientists using the system have access to all 96 unprocessed electrode waveforms enabling studies of neural activity as well as high quality spike sorting for identification and tracking of single neurons, a key feature used in both basic and applied neuroscience research [6].

The signal conditioning front end (Fig. 2) utilizes SC filtering to realize a band-pass characteristic. SC techniques usually suffer from a significant noise penalty due to foldback from sampling.

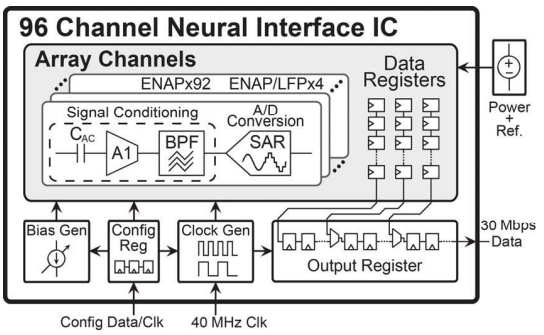

Fig. 1 Neural interface IC system diagram.

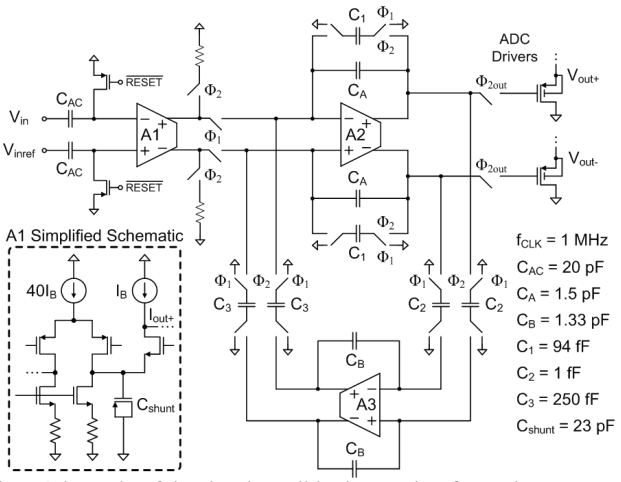

Fig. 2 Schematic of the signal conditioning section from Fig. 1.

However, in this design noise aliasing is mitigated through two steps of anti-alias filtering, allowing high noise efficiency. A1 is based on a folded cascode architecture with a scaled down output branch current (20:1) for low noise. A large subthreshold PMOS input pair is used to mitigate $1/f$ noise and is implemented with thick oxide devices to avoid bias shifts and noise from gate leakage. A 100 kHz dominant pole at the folding node is created by the added C_{shunt} capacitance, reducing the aliasing of wideband noise from the main current branch. Source degeneration is used to suppress both $1/f$ and wideband noise from the NMOS active loads, resulting in a relatively small thermal noise contribution from the resistances. During the Φ_1 phase, the combination of A1, A2 and C_B forms a Gm-C OTA integrator that samples the input signal. During Φ_2 the sampled charge is processed by A2 and A3 operating in feedback to implement a z-domain biquad transfer function. This filter topology is well known, though usually the instantaneous input voltage is sampled onto a capacitance in the input network of A2. In this design, integration of current during Φ_1 provides sinc filtering [7] for a second step of anti-aliasing. Sampling A1's output current with an integrator enhances power, noise and area efficiency; sampling A1's instantaneous output voltage onto an additional capacitor would degrade settling and contribute significant noise and area. This integrating current-mode sampling also has the fundamental advantage of reducing foldback of noise from A1's output branch devices without causing prohibitively slow dynamics at A1's outputs. Gain requirements on A2 are reduced by this sampling technique, allowing the use of a simple differential pair with SC CMFB. A3 is implemented as a two-stage miller compensated

OTA with SC CMFB (high gain and swing are needed in this amplifier's path to reject out-of-band signals). For simultaneous ENAP/LFP acquisition, A3 and the C_2 and C_3 switch clocks are turned off to disable the HPF pole, and the Φ_1 duty cycle is reduced to lower the gain. Subthreshold biasing was found to be optimal in the tradeoffs between transconductance efficiency, self-loading, and noise throughout the design, except in A1 where strong inversion is used in the output branch for low noise.

Low filter area allows the use of a 10-bit fully differential SAR ADC in each channel. Source followers are used to drive the 12 pF ADC input capacitances. Simulations indicate that the buffers achieve <0.01% settling error with a 100 kHz pole while each consumes less than 2% of the signal conditioning power per channel. The SAR ADC uses a fully differential 1-bit/9-bit split capacitor array with a 23.7 fF unit capacitance and a 2 unit series coupling capacitor [8]. SC CMFB networks in A1, A2 and A3 are refreshed during the A/D conversion cycle when the filter output need not be valid. The ADC data registers are daisy chained in 3 groups of 32 and pass data to an output register for shift-out during each conversion cycle. A configurable clock generator derives all the on-chip clocks from a 40 MHz external clock.

Measurements and Conclusion

The system was fabricated in TSMC's 0.13 µm mixed mode process (Fig. 3), and was used to record neural signals from a 100-channel Utah-style electrode array (Blackrock Microsystems) implanted in motor cortex of a rhesus macaque (Monkey L). All experiments and procedures were approved by Stanford's Institutional Animal Care and Use Committee. The recording quality was found to be on par with commercially available instrument grade recording systems (Cerebus, Blackrock Microsystems). 96 channels of ENAP signals and 4 channels of LFP are processed, acquired, and transmitted serially with a total power consumption of 6.5 mW from 1.2 V supplies and mid-supply references. Measured noise spectra and transfer functions for the ENAP and ENAP/LFP configured channels are shown in Fig. 4, obtained from a bench testing setup excluding the electrode array. Small differential mode artifacts from CMFB refresh result in the high frequency tones in the Fig. 4 noise measurements. These transients have mostly settled at the ADC sampling instant and are synchronously sampled, hence they are largely rejected. The noise measurements in Fig. 4 also contain 60 Hz tones and harmonics from minor power line interference in the test setup. The system's performance is summarized in Table I and compared to other recent neural interface designs (all systems are configurable and include different functions, typical recording performance is listed). The interface achieves higher fidelity acquisition (desirable for primate studies), and state-of-the-art power dissipation. The use of SC filtering results in a well-controlled filter response with good matching between channels and no need for tuning. [1-4] use gm-C filtering schemes that require hand tuning, have poor matching and sensitivity, and require large capacitances. [3, 4] employ multiplexed ADC architectures which save ADC area but increase complexity at the system level, whereas this work achieves a fine-grain pixel that relaxes system-level overhead and management, localizes analog signal processing, and contributes to a scalable architecture. Low voltage operation allows integration with a 1.2 V recording platform thereby enabling a system-level power reduction that [1-4] cannot provide.

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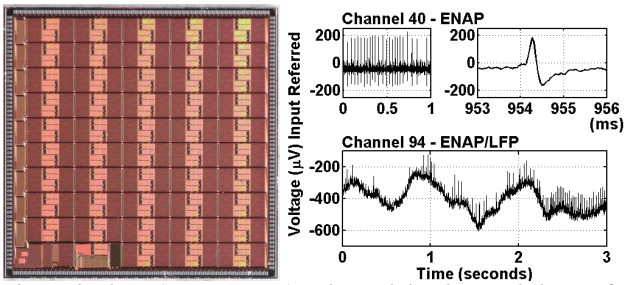

Fig. 3 Die photo (5 mm x 5 mm) and neural signals recorded *in vivo* from Monkey L showing action potentials (above) and simultaneous acquisition of action potentials and local field potential (below).

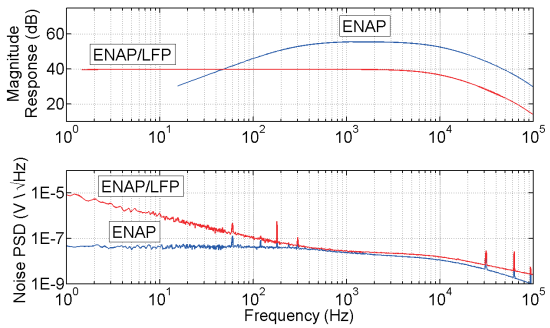

Fig. 4 Measured transfer functions and input referred noise spectra of the signal conditioning section.

TABLE I.

	This Work	[1]	[2]	[3]	[4]
VDD (V)	1.2	3.3	5	+/-1.65	3
Area (mm²)	25	25.4	discrete	63.4	8.5
Channels	96	100	32	128	128
Power (mW)	6.5	8	82	4.4	2.4
Bandwidth	10 kHz	5 kHz	5 kHz	20 kHz	5 kHz
Noise (µVrms)	2.2	4.8	3.2	4.9	6.08
ADC Resolution	10-bit	10-bit*	12-bit	9-bit	8-bit

*Only a single channel can be digitized at full bandwidth with this system.

References

[1] R.R. Harrison et al., "Wireless Neural Recording with Single Low-Power Integrated Circuit," *IEEE Trans. on Neural Sys. and Rehab. Eng.*, vol. 17, no. 4, pp. 322-329, Aug., 2009.

[2] H. Miranda et al., "HermesD: A High-Rate Long-Range Wireless Transmission System for Simultaneous Multichannel Neural Recording Applications," *IEEE Trans. on Bio. Circuits and Sys.*, vol. 4, no. 3, pp. 181, June, 2010.

[3] M. Chae et al., "A 128-Channel 6mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Transmitter," *ISSCC Dig. Tech. Papers*, pp. 146-603, Feb. 2008.

[4] F. Shahrokhi et al., "The 128-Channel Fully Differential Digital Integrated Neural Recording and Stimulation Interface," *IEEE Trans. on Bio. Circuits and Sys.*, vol. 4, no. 3, pp. 149, June, 2010.

[5] M. S. J. Steyaert et al., "A Micropower Low-Noise Monolithic Instrumentation Amplifier for Medical Purposes," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1163–1168, Dec., 1987.

[6] V. Gilja et al., "Autonomous Head-Mounted Electrophysiology Systems for Freely-Behaving Primates," *Current Opinion in Neurobiology*, vol. 20, no. 5, pp. 676-686, Oct. 2010.

[7] G. Xu and J. Yuan, "Comparison of Charge Sampling and Voltage Sampling," *Proc. of the IEEE MWSCAS*, pp. 440-443, Aug., 2000.

[8] Y.S. Yee et al., "A Two-Stage Weighted Capacitor Network for D/A-A/D Conversion," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 778-781, Aug., 1979.