A TECHNOLOGY FOR MONOLITHIC INTEGRATION OF HIGH-INDIUM-FRACTION RESONANT-TUNNELING DIODES WITH COMMERCIAL MESFET VLSI ELECTRONICS

R.J. Aggarwal, K.V. Shenoy, and C.G. Fonstad, Jr.

Department of Electrical Engineering and Computer Science
Research Laboratory of Electronics
Massachusetts Institute of Technology
Cambridge, MA 02139

ABSTRACT

A novel epitaxy-on-electronics (EoE) technology, developed at MIT, allows the integration of III-V heterostructures and commercial VLSI GaAs circuits. We have designed a monolithic resonant-tunneling diode- (RTD) based static random access memory which uses this technique. We review both the EoE process and the design and epitaxial growth techniques for high performance $In_xGa_{1-x}As/AlAs$ RTDs suitable for memories.

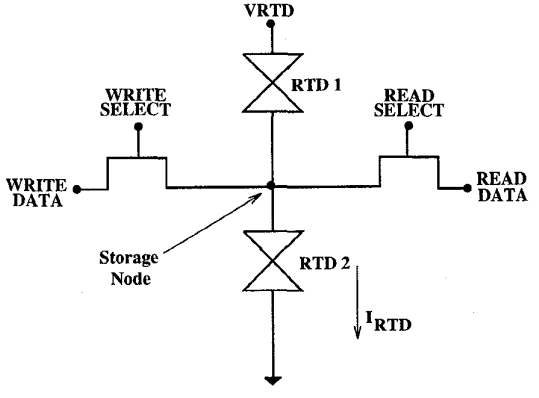

Figure 1: Schematic of an RTD/EFET SRAM cell.

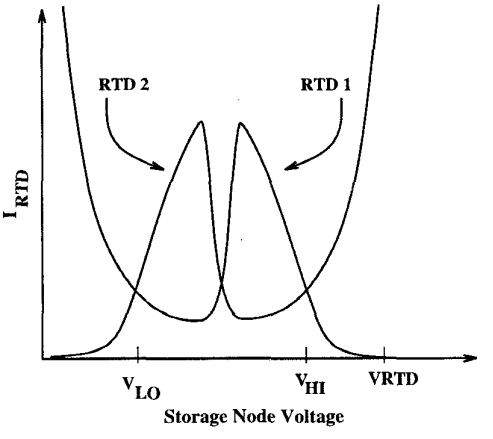

Figure 2: Load-line graph of the diode chain storage element.

1. INTRODUCTION

GaAs ICs have reached VLSI densities, but there remains a need for a compact GaAs SRAM cell. Demonstrations of SRAM cells built using III-V materials and based on resonant-tunneling diodes (RTDs) have been reported [1, 2]. However, the realization of a robust, VLSI-density integrated circuit technology based on reported integration techniques is uncertain. In work directed at optoelectronic integration, a novel epitaxy-on-electronics (EoE) technology has been recently developed at MIT [3, 4]. This technology enables the monolithic integration of III-V heterostructures and commercial VLSI GaAs circuits. This paper reports the design of a monolithic RTD-based SRAM cell employing commercial GaAs VLSI circuits.

2. RTD-BASED SRAM

A RTD-based SRAM cell offers potential area and power savings over traditional 6 transistor GaAs SRAM cells. Figure 1 shows a schematic of our memory cell. For demonstration purposes we have chosen a two transistor implementation. The RTD chain serves as a bistable storage element and the EFETs provide ac-

K.V. Shenoy supported by National Science Foundation and Fannie and John Hertz Foundation Graduate Fellowships.

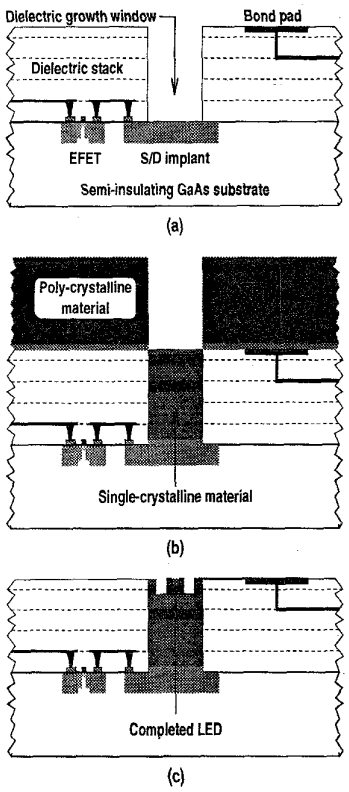

Figure 3: Schematic illustration of the EoE fabrication flow.

cess to the storage element. With additional READ-or-WRITE selection circuitry, the two-EFET architecture can be collapsed to a single-EFET topology. When optimized, this cell could require only the area of a single EFET. Figure 2 shows the electrical characteristics of the storage element. The static power requirements of the cell will be determined by the diode chain bias voltage, V_{RTD}, and the current flowing through the diode chain, I_{RTD}, in the V_{LO} and V_{HI} states. The speed of the READ and WRITE operations will primarily be determined by the diode and EFET abilities to charge the capacitance present at the storage node. Both the static power and speed of the cell are directly related to the RTD peak voltage, valley current, and the character of the diode initial turn-on current. For compatibility with DCFL voltage levels and optimum SRAM performance, we desire an RTD with a resonance voltage under 1 V, a sharp turn-on current, and large peak-to-valley-current ratio (PVCR).

3. EPITAXY-ON-ELECTRONICS TECHNOLOGY

The EoE technology, shown in Figure 3, places time-temperature constraints on our epitaxial process. Targeting VLSI densities of electrical and heterostructure

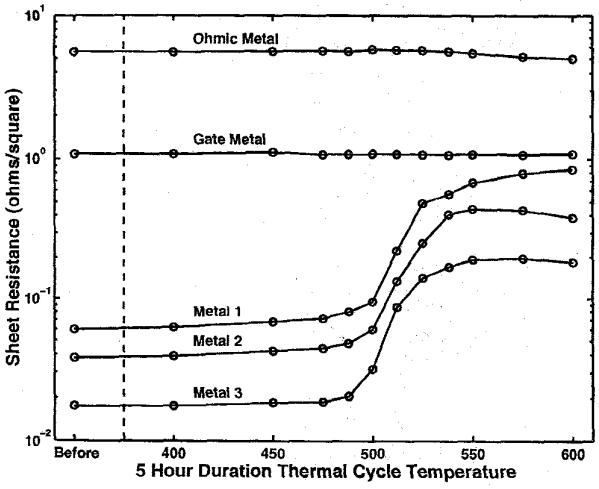

Figure 4: Metal layer sheet resistance after 5 hour thermal cycles. At elevated temperatures a metallurgical reaction, $AlCu_x + WN_x \rightarrow$ Al-Cu-W-N, occurs within the interconnect metal layers which increases the sheet resistance.

devices, our starting point is commercial VLSI GaAs metal-semiconductor field-effect transistor (MESFET) circuitry available at foundries such as Vitesse Semiconductor Corp. through the MOSIS/ARPA service. By overlaying existing standard foundry process etches it is possible to specify dielectric growth windows (DGWs) during circuit layout as illustrated in Figure 3(a). The second fabrication step, seen in Figure 3(b), is to epitaxially grow heterostructures on the fully-processed commercial electronics-only GaAs wafer or chip. Single-crystal, device-quality material grows from the GaAs wafer to the top of the interlevel-metal dielectric stack (DGW sidewalls) in the DWGs while poly-crystalline material deposits on the dielectric stack. The poly-crystalline deposits are then removed and heterostructure devices are fabricated with standard processing techniques. The final fabrication step connects the heterostructure devices, an LED in the case of Figure 3(c), and the GaAs circuits.

The heterostructure growth time-temperature upper limit is set by the thermal stability of the underlying electronics. In our studies of the stability of GaAs electronics we have investigated the HGaAs2 [5] and HGaAs3 [6] processes of Vitesse Semiconductor Corp. and the CS-1 process of Motorola. Both lines produce VLSI density, 0.5 μm gate width GaAs E-mode and D-mode MESFETs with refractory metal gates (tungsten-nitride based) and ohmic contacts (nickel based) while interconnect wires are aluminum-copper plated with tungsten-nitride. The ohmic contacts are stable to ap-

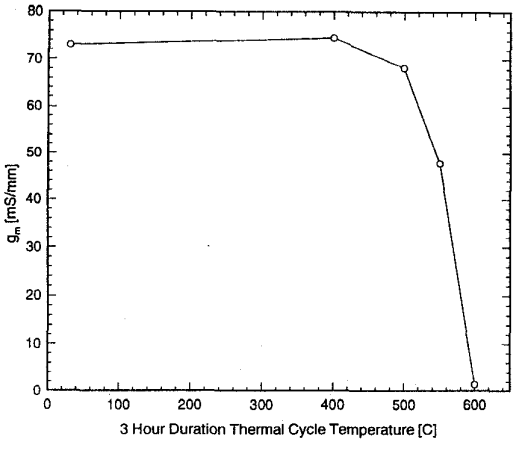

Figure 5: The maximum transconductance, g_m (V_{DS} = 0.15 V), of fully processed 50 μm x 1.2 μm gate E-mode MESFETs after 3 hour anneals at temperatures between 400°C and 600°C.

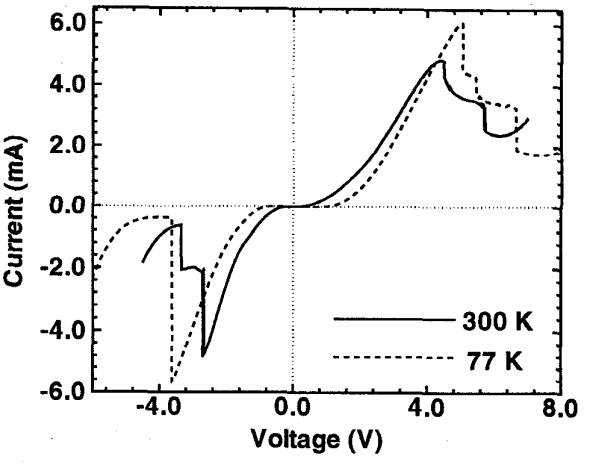

Figure 6: Current-voltage characteristics of a typical 25 μm^2 $In_{0.22}Ga_{0.78}As$/AlAs relaxed-buffer RTD.

proximately 500°C for three hour thermal cycles. Figure 4 shows the sheet resistance of the various circuit metals as a function of thermal cycle temperature. The GaAs intrinsic transistors are stable to much higher temperatures. Figure 5 shows the transconductance of E-mode MESFETs as a function of thermal cycle temperature. We have shown that the thermally-weak link in the circuits is the multi-layer metal film used in the upper-level interconnect lines, which typically limits epitaxy temperatures to below 475°C growth times to below 5 hours.

4. RELAXED-BUFFER RTDS

The PCVR of GaAs/$Al_xGa_{1-x}As$ RTDs grown on GaAs can be improved by replacing GaAs with $In_xGa_{1-x}As$. $In_xGa_{1-x}As$ critical thickness limits restrict the indium content of the $In_xGa_{1-x}As$, and therefore limit the utility of this approach. By using a strain-relieved buffer, the substrate lattice constant can be changed to match that of the diode $In_xGa_{1-x}As$ layers. We are using this approach to design RTDs suitable for circuit applications.

We use a two-step relaxed buffer to grow high-indium-composition RTDs compatible with the EoE technology. We have recently demonstrated a $In_{0.22}Ga_{0.78}As$/AlAs relaxed-buffer RTD with a PVCR of 13:1 [7]. The relaxed buffer consists of 0.55 μm of $In_{0.17}Ga_{0.83}As$ and 0.32 μm of $In_{0.22}Ga_{0.78}As$ both n-type. The $In_xGa_{1-x}As$ layers were grown at 480°C and total growth time was 3 hours. Figure 6 shows the electrical characterization of the device. The resonance voltages in this structure are high due to low buffer and RTD doping concentrations and a narrow RTD well width and are too large to be useful in SRAM cells.

To determine the contribution of the relaxed buffer to the resonance voltage of the RTD, several relaxed-buffer RTDs were grown. Once again, a two-step relaxed buffer grown at 480°C was used. The electrical characteristics were measured using two different four-point probe configurations. For both measurements, the "top" contact of the RTD was the ohmic contact on the RTD mesa. The "bottom" contact was the substrate in one case, and an ohmic contact above the relaxed buffer in the other. The difference in the peak voltage represents the voltage drop across the buffer. Figure 7 shows the I-V characteristics of an $In_{0.27}Ga_{0.73}As$/AlAs relaxed-buffer RTD. The relaxed buffer for this RTD consists of 0.2 μm $In_{0.11}Ga_{0.89}As$ and 0.2 μm $In_{0.27}Ga_{0.73}As$, both doped n^+. The resonance voltage of this diode is lower than that of Figure 6 because of higher buffer and RTD doping and a wider RTD well. The relaxed buffer voltage drop for this diode, under 30 mV, can be accounted for in future RTD designs. In general, RTDs with heavily doped relaxed buffers are suitable for circuit applications.

5. MONOLITHICALLY INTEGRATED RTD-BASED SRAM DESIGN

Large signal design parameters from relaxed-buffer RTDs were used to design three basic circuits which study the feasibility of integrating RTDs with GaAs ICs: an RTD array, a 1-bit memory cell, and a 4-bit memory array. The RTD array is used to study the quality of the RTD material grown on the GaAs ICs.

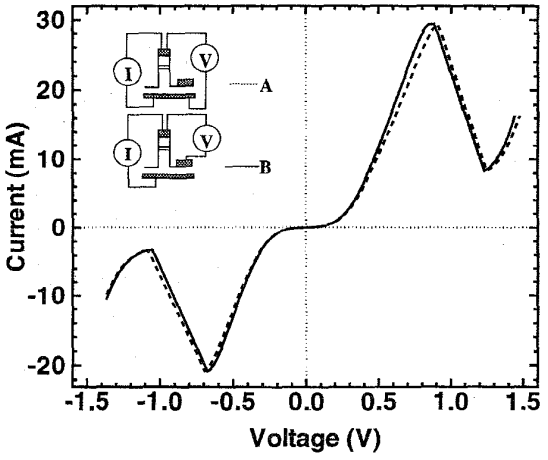

Figure 7: Current-voltage characteristics of a typical 25 μm^2 $In_{0.27}Ga_{0.73}As$/AlAs relaxed-buffer RTD including and excluding the voltage drop contributed by the relaxed buffer.

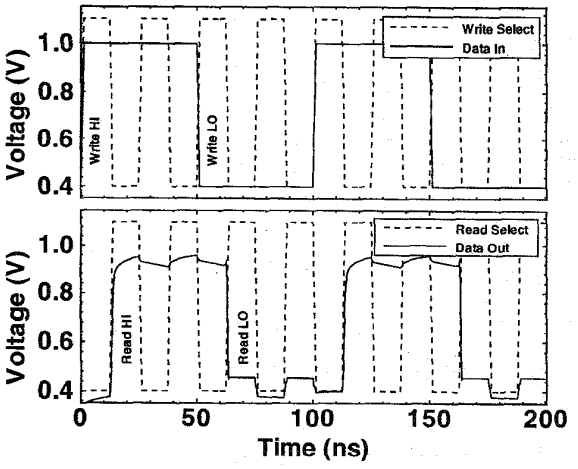

Figure 8: Simulated operation of 1-bit SRAM cell.

The 1-bit memory cell characterizes the basic operation of the memory cell. The 4-bit memory array addresses density issues such as the effect of RTD variation on the performance of the memory. Figure 8 shows the simulated operation of a 1-bit memory cell using layout extracted EFET characteristics. The RTDs used in this simulation are those shown in Figure 7. The *Select* signals are applied to gates of the EFETs and the *Data In* signal is applied to the drain of the WRITE EFET shown in Figure 1. The *Data Out* signal is measured at the drain of the READ EFET.

6. CONCLUSION

We have designed a RTD-based SRAM utilizing a novel EoE technology to combine III-V heterostructures with commercial VLSI GaAs circuits. Upper epitaxial time-temperature limits are set by the metal interconnects. Operating within these constraints, we use a relaxed-buffer structure to epitaxially grow high-indium fraction RTDs on GaAs substrates which are compatible for circuit applications. We are presently fabricating the monolithically integrated SRAM circuits.

This work was supported by JSEP through the MIT Research Lab of Electronics and ARPA through the National Center for Integrated Photonics Technology.

7. REFERENCES

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