W3.4 (Invited)
3:10pm - 3:40pm

Application Specific OEICs Fabricated using GaAs IC Foundry Services

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A novel epitaxy-on-electronics process for fabricating optoelectronic integrated circuits (OEICs) with high performance optoelectronic devices monolithically integrated with VLSI density and complexity GaAs electronic circuitry has been proposed, demonstrated, and continues to be developed by a research team[1] at MIT associated with the ARPA-funded National Center for Integrated Photonics Technology (NCIPT)[2] and working in collaboration with other researchers at Caltech[3], GTE Labs Inc.[4], MIT Lincoln Laboratory[5], Motorola, Inc.[6], and Vitesse Semiconductor Corp.[7]. Building on the existing commercial gallium arsenide integrated circuit technology base, this epi-on-electronics approach does not require the development of a VLSI electronics technology, unlike the more common epitaxy-first approach. It thus promises to provide a direct, immediate route to the realization of large-scale application-specific OEICs for a variety of applications.

Recent work by researchers at MIT has shown that gallium arsenide MESFETs fabricated using commercial VLSI processes incorporating refractory metal ohmic contacts and gates, and standard (Si IC-like) back-end multi-level dielectric and interconnect technology, are not adversely effected by several hours at elevated temperatures[8]. This means that these devices will survive the molecular beam epitaxy growth sequence for many III-V optoelectronic device heterostructures. In fact, these MESFETs still function after being annealed at as high as 700°C, but as Figure 1 illustrates, the room temperature characteristics change for anneals above 500°C. Thus if established design rules and simulation tools are to be used, the bulk of the epitaxial growth run must be conducted at 500°C or less.

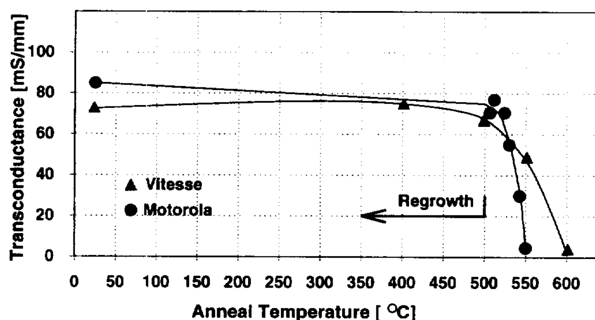

Figure 1: The room temperature transconductance of GaAs enhancement-mode MESFETs after 3 hour anneals at the temperatures indicated. This data was measured on standard test bars included on fully processed VLSI wafers fabricated by Vitesse and Motorola.

Most epitaxy on GaAs, particularly of AlGaAs heterostructures, is done in excess of 600°C and restricting the growth temperature to under 500°C is indeed an issue, particularly for laser diodes, the most demanding of all optoelectronic devices. Fortuitously, lowered-temperature growth

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[8]K.V. Shenoy, C.G. Fonstad Jr., and J. Mikkelson, *IEEE Electron Dev. Lett.* 15 (1994) 106-108.

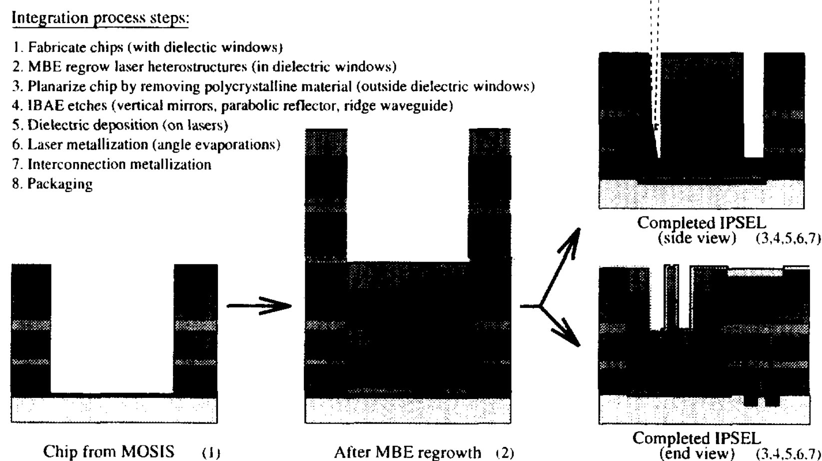
is a topic that has coincidently received considerable attention recently and there have been several reports of high performance AlGaAs laser diodes grown by molecular beam epitaxy at under 500°C[9]. Even more exciting have been developments using InGaP wide-bandgap layers to replace AlGaAs in GaAs-based optoelectronic devices; thresholds as low as 72 A/cm^2 have been reported for InGaP/InGaAs/GaAs laser diodes grown for the most part at 500°C[10].

Based on the above results, Shenoy et al. at MIT[11-12] have developed processes to do MBE regrowth in windows opened through the dielectric layers on processed VLSI circuits, to remove the polycrystalline deposits on the dielectric and planarize the wafer surface, and to process the epitaxial heterostructures into diode lasers and light emitting diodes monolithically integrated with, and electrically connected to, the commercially processed electronics. Figure 2 illustrates this process by showing cross-sectional views of an in-plane surface-emitting laser (IPSEL)[13] at several stages in the process sequence.

The regrowth and post-epitaxy processing techniques developed at MIT have been used in collaboration with Grot et al. at Caltech to integrate light emitting diodes with a variety of neural network circuits obtained through the MOSIS service[14-15]. These circuits have incorporated back-side contact to the LEDs through the source-drain contact implant and monolithic electrical integration using metal lines running over the dielectric-heterostructure boundary, and demonstrate the feasibility of the MIT epi-on-electronics process. Another set of chips, also obtained through MOSIS and containing optoelectronic transceivers, is being used in the development of epi-on-electronics processes for IPSELs.

Other work in progress includes research on compact fiber-coupled (as well as surface-normal) components in this technology, on low-temperature solid-source MBE growth of AlGaAs/InGaAs/GaAs and gas-source MBE growth of InGaP/InGaAsP/GaAs laser diode and guided-wave optical device heterostructures, and on the design of additional application-specific OEICs using the epi-on-electronics process.

Figure 2: Cross-section views of an epi-on-electronics OEIC IPSEL at several points in the process: Left - As received from the GaAs IC manufacturer with all electronics processing complete and with windows for epitaxy open; Middle - After MBE regrowth with epitaxial heterostructure on the exposed substrate and polycrystalline deposit on the dielectric layers; Right - Completed IPSEL with electronics viewed from the side (top) and end-on (bottom).



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