Integration of LED's and GaAs Circuits by MBE Regrowth

Annette C. Grot, Demetri Psaltis, Krishna V. Shenoy, and Clifton G. Fonstad, Jr.

Abstract—**Fully processed VLSI GaAs MESFET circuits, available through the MOSIS service, have recently been shown to be electrically stable after 3-h thermal cycles at 500°C. It is therefore feasible to epitaxially regrow photonic device heterostructures directly on high-density electronic circuits yielding monolithic optoelectronic VLSI circuits. The MBE growth, planarization, and LED fabrication of the first optoelectronic circuit using this novel integration technique are described.**

THE uniformity required for large two-dimensional optoelectronic arrays can only be achieved with state-of-the-art technology available at an industrial foundry. In fact, one of the main reasons for the slow development of large-scale two-dimensional optoelectronic arrays is the lack of an industrial foundry for optoelectronics similar to the existing foundries for electronic silicon circuits. Since there is currently no commercially available foundry for custom-designed optoelectronic circuitry, several groups have built hybrid optoelectronic arrays by taking advantage of an existing foundry for the electronic circuitry and attaching hybrid optical devices afterwards [1], [2]. In this paper we describe how GaAs optical devices can be monolithically integrated with GaAs MESFET-based circuitry fabricated by Vitesse Semiconductor Co. through MOSIS [3].[1] The fully processed GaAs circuits from MOSIS can withstand temperatures up to $525° \pm 10°C$ for 3 h without significant changes in performance [4], and therefore it is possible to regrow heterostructures on such circuits to monolithically integrate optical devices such as multiple quantum well (MQW) modulators, light emitting diodes (LED's) and laser diodes.

The most general optoelectronic circuit consists of photodetectors, electronic circuitry, and some form of optical output, either an optical source or an optical modulator. The process provided by MOSIS/Vitesse allows one to design circuits with enhancement-mode (threshold voltage, $V_T = 0.27$V) and depletion mode ($V_T = -0.65$V) MESFET's, Schottky diodes, as well as photodetectors [3]. The electronic circuit component of the optoelectronic circuit can be designed using standard CAD design and layout tools. The regrowth region is allocated by leaving blank areas where there is no electronic circuitry in the chip design and ultimately removing the dielectric layers in these regions so that the wafer surface is exposed. Fig. 1 shows the chip cross section of the optoelectronic circuit. The transistor circuits are ion-implanted GaAs MESFET circuits with tungsten-based refractory metal Schottky gates, nickel-based refractory metal ohmic contacts, and three levels of aluminum interconnect metallization. Two of the metal levels are used for signal routing and the third for power distribution. The total thickness of the dielectric stack, used to separate the various aluminum interconnect metal, is approximately 4μm. To determine the uniformity of the MESFET's, the drain–source current of 20 depletion-mode MESFET's ($L = 2.8\ \mu$m, $W = 13.6\ \mu$m) was measured with the gate voltage kept constant ($V_{gs} = 0$ V). The average current was 250 μA, and the standard deviation was 15 μA, which corresponds to a 6% uniformity.

In the present circuit, the photodetectors are enhancement-mode MESFET's. When light is incident in the gate region, carriers are created, which changes the conductance of the channel. An enhancement-mode MESFET with its gate tied to its source ($V_{gs} = 0$ V) will conduct very little current when no optical signal is present. Under illumination, the MESFET behaves as if a positive voltage were applied to the gate. Fig. 2 shows the I–V characteristics of an enhancement mode FET ($L = 2.8\ \mu$m, $W = 13.6\ \mu$m) with its gate tied to its source at different illumination intensities ($\lambda = 840$ nm, beam diameter $= 25\ \mu$m). This high responsivity is typical for dc detection of light in optical FET's.

Single crystal GaAs epitaxial layers were regrown in the regrowth regions on the chips by solid source MBE. It was decided to integrate LED's with the MOSIS/Vitesse circuitry because LED's allow one to work with small currents so that a higher density can be achieved than would be possible with laser diodes [5]. For this particular circuit layout, half of the MOSIS/Vitesse chip was left blank for the regrowth and the other half contained the MESFET circuitry. The first step in the LED regrowth process was to remove the dielectric stack covering the area on the chip allocated to the LED's. The circuits were covered with wax and the dielectric stack was etched with HF. It is possible to have the openings lighographically defined at the foundry [6], [7]. Once the dielectrics were removed, the chip was degreased and placed

Manuscript received November 16, 1993; revised April 27, 1994. This work was supported in part by ARPA through NCIPT at M.I.T. and OMC at the California Institute of Technology, in part by the National Science Foundation through graduates fellowships to A. C. Grot and K. V. Shenov, and in part by the Fannie and John Hertz Foundation through a graduate fellowship to K. V. Shenov.

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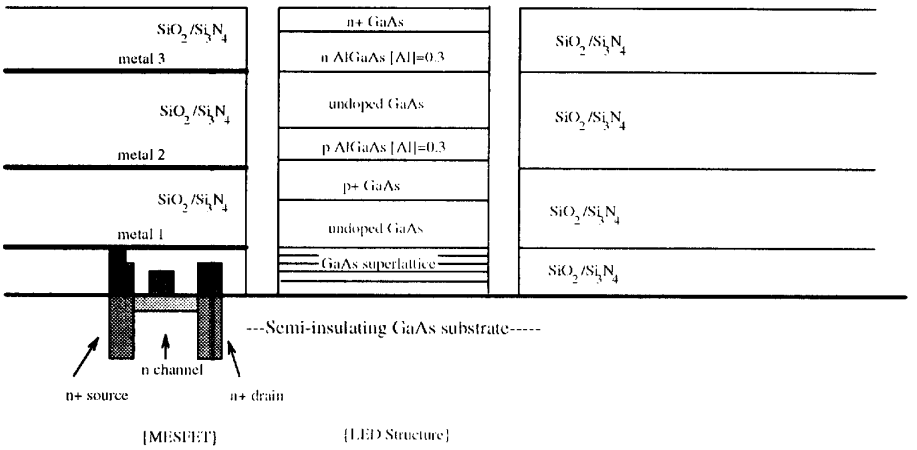

Fig. 1. Cross-section of MOSIS/Vitesse chip with an LED structure monolithically integrated by MBE regrowth. Double heterostructure LED material is grown in areas where there are no circuits.

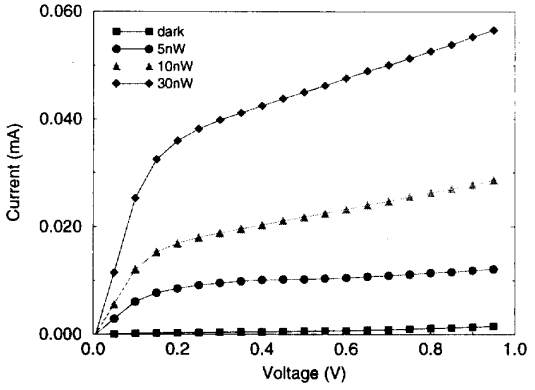

Fig. 2. I–V characteristics of an enhancement-mode FET with different light intensities illuminating the gate region. The optical source was an AlGaAs/GaAs laser diode operating at 840nm. The responsivity of this device at 10nW is determined to be 1800 A/W.

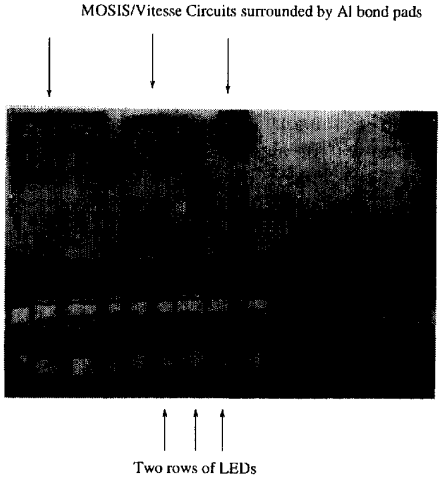

Fig. 3. Photograph of the MOSIS/Vitesse chip showing the MESFET's circuits and the LED regrowth area. The electronic circuits are on the left side of the photograph and the LED's are on the far right side.

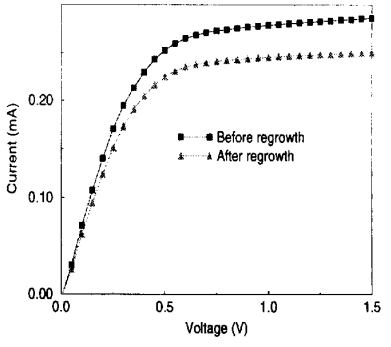

Fig. 4. I–V characteristics of a depletion-mode FET before and after MBE regrowth. ($V_{gs} = 0$V, $L = 2.8\mu$m, $W = 13.6\mu$m).

in the MBE chamber. The epitaxial structure grown is shown in Fig. 1. The superlattice was grown to impede upward propagation of defects from the semi-insulating substrate. The total growth time was nearly 4 h at the lowered growth temperature of 530°C. The polycrystalline GaAs that covers the circuits on the chip was removed by masking off the crystalline GaAs with photoresist and then etching with a phosphoric etchant (1:1:5 H_3PO_4:H_2O_2:H_2O), which does not significantly attack the aluminum pads of the circuit. The final steps were an etch of the crystalline GaAs to form the LED mesa structures and evaporation of the n (AuGe/Ni/Au) and p (AuZn/Au) ohmic contacts. Connections between the LED and the MESFET circuitry can be made either externally or by depositing interconnect metal. In the experiments shown below, the connection was made externally. A photograph of the completed optoelectronic chip is shown in Fig. 3. The cracks visible over the circuits are in the top dielectric overglass layer and did not interfere with the operation of the circuits underneath. They can be minimized by reducing the MBE substrate temperature ramp rate.

In order to determine the degradation in the MESFET circuits due to exposure to high temperature for a prolonged

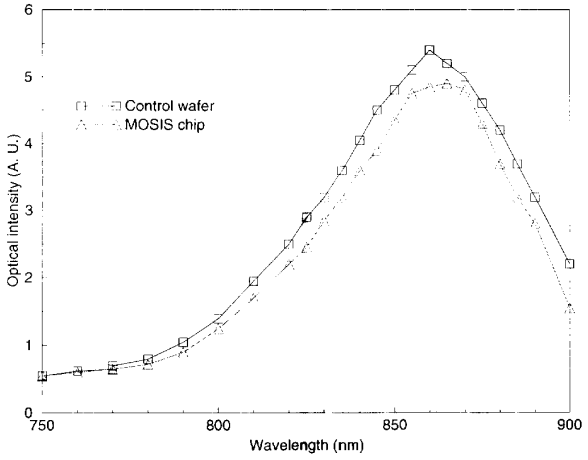

Fig. 5. Photoluminescence from a blank control wafer and the MOSIS/Vitesse chip after regrowth.

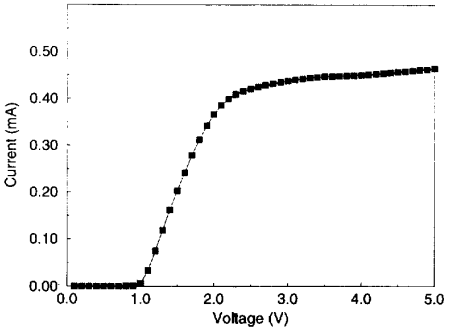

Fig. 6. The current through the LED and depletion-mode MESFET when connected in series as a function of the voltage applied across the circuit.

period, the circuits were electrically tested after the growth and their performance was compared with that of the original circuit. Fig. 4 shows the before and after I–V curves for a depletion MESFET with its gate connected to the source. The saturation voltage is the same, whereas the saturation current has decreased by approximately 10%, and the source-to-drain resistance has increased by 40%. The specific degradation mechanism is currently being investigated [4].

After the electrical testing of the circuits fabricated by MOSIS/Vitesse, the photoluminescence of the epitaxial material was measured and compared with the photoluminescence of a blank GaAs wafer (semi-insulating, epi-ready wafer from AXT Corp.) that was grown at the same time. As shown in Fig. 5, the strength of the photoluminescence is comparable for the two wafers. LED's were fabricated on the chip, as well as on the control wafer, without current confinement. The efficiencies obtained were low (0.01% at 100μA and 0.03% at 1mA) due to the lack of current confinement. The efficiency is approximately the same on the control wafer. Similar LED's grown at 700°C and identically processed had nearly identical I–V curves and equally low efficiencies, confirming that the low efficiencies were inherent in the structure and are not due to the integration technique. Fig. 6 shows the I–V characteristics of the LED in series with the DFET.

This new method of integrating optical devices with commercially available custom designed MESFET circuitry allows the system designer to design complex optoelectronic circuits and arrays with fast turn-around time and little capital investment. The dielectric etch can actually be incorporated into the Vitesse process. Furthermore, by growing the LED structure n-side down on a source/drain ion-implanted n^+ region, the n contact of the LED can be directly made to the MESFET circuitry [6], [7]. Thus the only processing steps needed after regrowth are one etch to remove the polycrystalline GaAs, define the LED active region, and the p-contact evaporation.

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