11:30am - 11:45am
EOS/OTA2.4

Room 207

Laser Diodes and Refractory-Metal Gate VLSI GaAs MESFETs for Smart Pixels†

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We demonstrate for the first time that VLSI GaAs wafers can withstand the time-temperature cycles encountered during the growth and processing of high performance laser diodes, and demonstrate for the first time key process and device elements of a sequence for integrating optoelectronic devices on fully processed VLSI GaAs circuits.

Smart pixels, advanced image processors, and optical interconnect schemes all require the integration of optoelectronic devices with VLSI-level electronic circuitry. Optoelectronic devices are best made in the III-V semiconductors. Early GaAs technologies, however, could not withstand a post-process epitaxial growth sequence; nor were they at VLSI levels. Thus research on OEICs has been directed at integrating GaAs on Si VLSI, or at developing entirely new III-V technologies based on complex multiple epilayer stacks. In this paper it is demonstrated that current refractory-metal gate, gold-free processes are unaffected by molecular beam epitaxy (MBE) growth, and that growth on VLSI GaAs is a viable approach. By building on an existing GaAs technology base, the VLSI levels of integration required to make complex OEICs viable are immediately available, and research efforts can be focused on optimizing the optoelectronic devices.

Fully processed VLSI GaAs wafers, and similar wafers processed only through ohmic and gate metal deposition, were annealed in a hydrogen atmosphere to temperatures between 400 and 700°C for periods up to 5 hours to simulate MBE growth cycles. Subsequent measurements on enhancement and depletion mode MESFETs and on a variety of test structures show that functional devices remain after all anneals (Fig. 1), and that there were no significant changes in the Schottky barrier gates or in the ohmic contacts (Fig. 2). More importantly, there are negligible changes in any device parameters on fully processed wafers up to 530°C (Figs. 3,4). Thus if laser heterostructures can be grown and processed without exceeding 530°C, no modification of IC design rules is required; this is an extremely important result.

Single quantum-well, step-confinement, strained-layer (Al,Ga,In)As laser diode heterostructures were optimized for growth at low temperatures. Low Al mole fraction cladding layers, 1.4 μm $Al_{0.22}Ga_{0.78}As$, minimized oxygen incorporation at heterojunction interfaces and allowed ridge waveguide lasers to be fabricated using a selective succinic acid etch and an AlAs etch-stop layer. 200 nm GaAs waveguide layers maximized the optical confinement factor and maximized the quantum well to AlGaAs cladding layer separation which is critical with low temperature AlGaAs[4]. A 60 Å $In_{0.2}Ga_{0.8}As$ active region minimized threshold currents and nominally emitted at 0.98 μm. Such laser diodes were MBE grown with a maximum substrate temperature of 530°C and had threshold current densities only 2.4 times higher than lasers grown under more optimal growth conditions. This demonstrates for the first time that practical laser diodes can be grown using standard MBE techniques at temperatures compatible with direct epitaxial growth on fully processed VLSI GaAs circuitry. Further reduction in threshold currents are anticipated and preliminary selective area (patterned) growth studies have been conducted.

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[4]S. Win, K.F. Longenbach, and W.I. Wang, *Electronics Letters*, 27(3):199-200, 1991

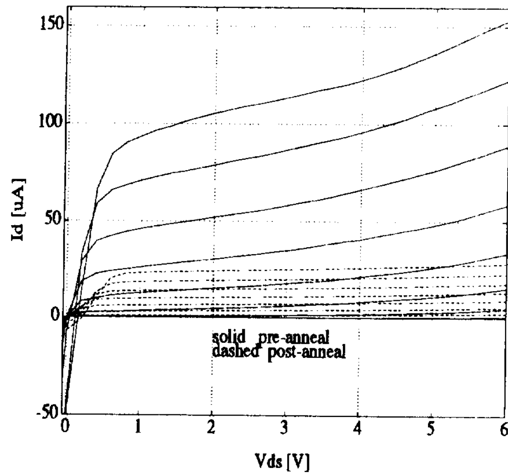

Figure 1: Transistor functionality is retained after a 700°C, 5 hour anneal. Measured on 1.5 × 1.2 μm partially processed EFET with V_{gs} increased from 0 to 0.8 V.

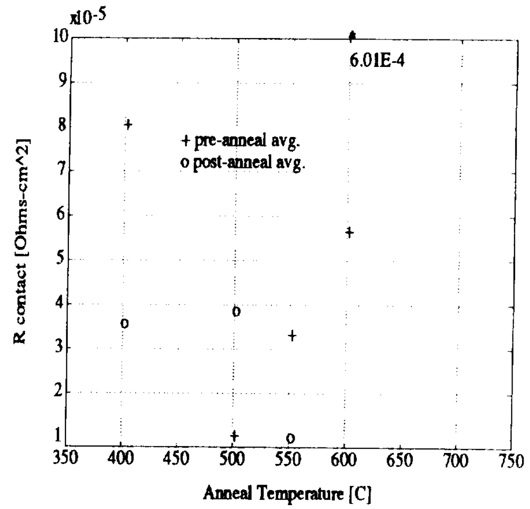

Figure 2: Source and drain contact resistance are not significantly altered after 3 hour anneals. Measured on fully processed transmission line model (TLM) structures.

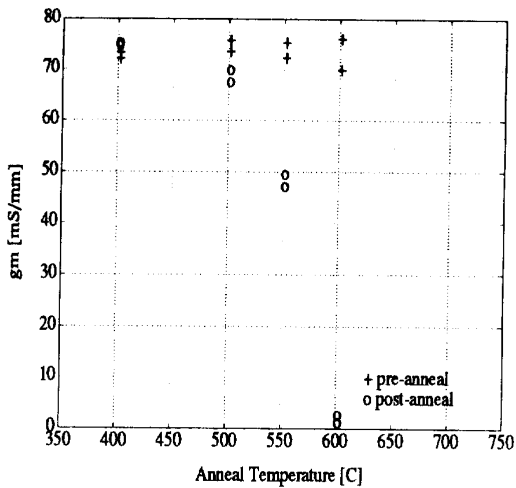

Figure 3: Maximum transconductance, g_m, decreased significantly after 3 hour anneals above 530°C. Measured on 1.5 × 1.2 μm fully processed EFET with V_{ds}=0.15 V

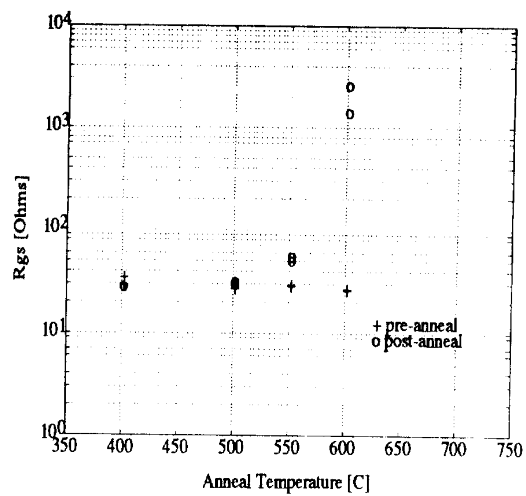

Figure 4: Gate to source series resistance, R_{gs}, increased significantly after 3 hour anneals above 530°C. Measured on 1.5 × 1.2 μm fully processed EFET with I_{ds}=10 μA