4:30pm - 4:45pm
OM2.3 **Room C2**

Optoelectronic VLSI Circuit Fabrication[†]

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We demonstrate for the first time key components of a fabrication sequence for immediately manufacturing monolithic optoelectronic very large scale integration (OE-VLSI) circuits and systems. Commercially available, self-aligned VLSI GaAs MESFETs, with tungsten-based refractory metal Schottky gates, nickel-based refractory metal ohmic contacts, and aluminum interconnection metallization, have recently been shown to be stable after more than 4 hours at 525 $\pm$ 10°C[4,5]. Thus, it is now possible to regrow optical sources, detectors, and modulators on fully processed MESFET circuitry. VLSI circuits and systems can, therefore, be built with optical inputs and optical outputs without electronic circuit design rule modification. Such OE-VLSI circuits and systems are useful for high speed optical communication and optical computing (smart pixels).

An OE-VLSI circuit can be fabricated in four steps: 1) foundry fabrication of the electronic circuit design, 2) selective epitaxial regrowth of photonic heterostructures in window regions (GaAs substrate exposed), 3) removal of inter-window polycrystalline material and photonic device processing, and 4) photonic and electronic device interconnection (Table 1). By cascading these mature technologies, high performance OE-VLSI circuits are immediately available.

Recently, a first generation optoelectronic neuron array was fabricated demonstrating the integration of LEDs with VLSI GaAs MESFETs[6,7]. Each neuron consisted of two phototransistor inputs, nonlinear thresholding electronics, and a LED output (Fig. 1). The desired optoelectronic thresholding function was achieved while maintaining good electronic circuit performance and LED efficiencies.

Based on this initial success, an OE transceiver (generic smart pixel) was designed, regrown, and is nearing completion to demonstrate the high-density integration of LEDs, ridge lasers, and in-plane surface emitting lasers (IPSELs) with state-of-the-art VLSI GaAs MESFET transceiver designs. Each transceiver is approximately 0.4 mm^2 and consists of an ECL electrical input receiver and output driver, an MSM photodetector with a companion transimpedance amplifier, a cross point switch, control logic, and two windows for epitaxial regrowth (Fig. 2). IPSELs are attractive for the following reasons: 1) $V_{th} < 2$ V is compatible with DCFL MESFET logic levels, 2) heterostructure thickness ≈ 4 μm is planar with electronics, 3) low divergence angles (13° $\perp$ FWHM)[8], and 4) η_d as high as 66% pulsed and 48% cw[9]. Fig. 3 is an optical and scanning electron micrograph of selectively grown strained-layer (Al,Ga,In)As laser heterostructures in which vertical mirror facets, a parabolic deflection mirror, and a ridge waveguide have been fabricated using chlorine ion-beam-assisted etching. Electronic circuitry is also clearly shown in Fig. 3, which is an indication of the robustness of the planarization and polycrystalline removal technique. Preliminary characterization of completed OE-VLSI transceiver circuits will be presented.

[†]Work at MIT supported by ARPA through NCIPT. Work at MIT Lincoln Laboratory supported by the Department of the Air Force.

[1]Supported by National Science Foundation and Fannie and John Hertz Foundation Graduate Fellowships.

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[5]K.V. Shenoy, C.G. Fonstad, Jr., and J.M. Mikkelson, submitted to IEEE Electron Device Letters.

[6]A.C. Grot, D. Psaltis, K.V. Shenoy, and C.G. Fonstad, Jr., OSA 1993 (Palm Springs, CA), March 1993.

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[8]J.P. Donnelly, W.D. Goodhue, et al., *Appl. Phys. Lett.*, **61** (13), 28 Sept. 1992.

[9]J.P. Donnelly, W.D. Goodhue, et al., submitted to IEEE Photonics Technology Letters.

#	Step Description
1	Electronics Circuit design Standard GaAs MESFET design rules Circuit fabrication Commercial foundry, MOSIS/Vitesse
2	Epitaxial Regrowth of Photonics Window clean RIE and wet chemical Molecular beam epitaxy (MBE) Lowered-temperature (Al,Ga,In)As growth
3	Photonics Chip planarization Polycrystalline material removal Device fabrication Standard photonic device processing
4	Interconnection Optical and electrical device connection Gold-based metallization

Table 1: OE-VLSI fabrication sequence followed for demonstration projects.

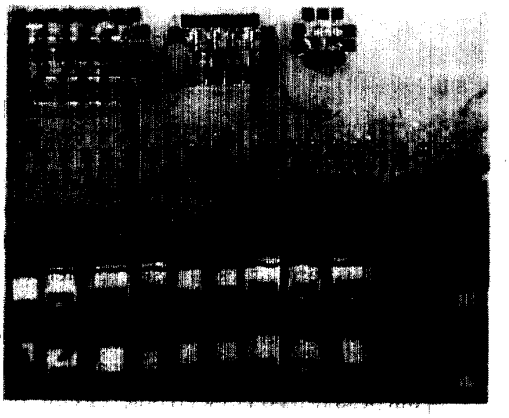

Figure 1: First generation neural array consisting of GaAs MESFETs (top) and double heterostructure (Al,Ga)As LEDs (bottom).

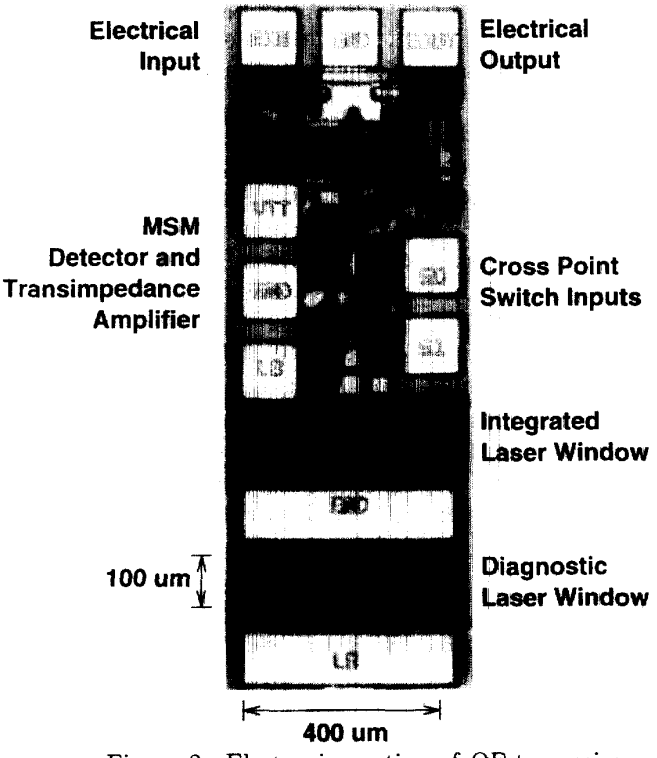

Figure 2: Electronic portion of OE-transceiver as received from foundry consisting of VLSI GaAs MESFETs (top) and windows exposing substrate (bottom). Each OE transceiver is approximately 0.4 mm^2.

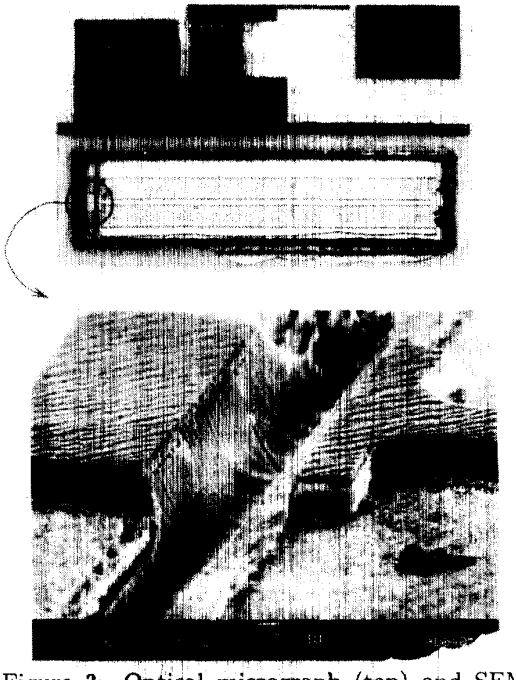

Figure 3: Optical micrograph (top) and SEM (bottom) of selectively grown strained-layer (Al,Ga,In)As laser heterostructures in which vertical mirror facets, a parabolic deflection mirror, and a ridge waveguide have been fabricated using chlorine ion-beam-assisted etching. Electronic circuitry is also clearly shown, which is an indication of the robustness of the planarization and polycrystalline removal technique. Fabrication improvements are expected.