Monolithic Optoelectronic VLSI Circuit Design and Fabrication for Optical Interconnects

by

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Abstract

Optical interconnects (OIs) offer solutions to several inherent electrical interconnect performance limitations. Reduced cross talk, lower drive powers, higher bandwidths and optional transmission media enable OIs to achieve superior performance with both existing and new interconnect architectures. OIs consist of optical emitters or modulators, optical detectors and associated electronic circuitry. Large-scale high-density OI systems require the monolithic integration of optical and electrical devices, forming optoelectronic integrated circuits (OEICs). At present, OI systems are limited by the inability to fabricate VLSI-level OEICs. A novel optoelectronic integration technique capable of producing VLSI OEICs was proposed, developed and demonstrated in this work.

The Epitaxy-on-Electronics (E-o-E) optoelectronic integration technique involves epitaxial growth of optical device heterostructures on fully processed VLSI GaAs MESFET electronic circuits. A commercially available, refractory-metal enhancement- and depletion-mode MESFET process was shown to be stable after 5 hour, 470°C molecular beam epitaxy (MBE) growths with intrinsic devices surviving beyond 5 hours at 525°C. Based on this thermal stability, circuits were designed and commercially fabricated to serve as the OEIC electronics. The electronic circuits GaAs substrate also serves as the optical device substrate. During circuit design, openings through the interlevel dielectric stack to the GaAs substrate, termed dielectric growth wells (DGWs), were also specified by stacking two standard process etch layers. Optical device heterostructures were grown on the chips by MBE at lowered growth temperatures resulting in epitaxial material in the DGWs (epi-islands). The poly-crystalline material in the inter-DGW regions was removed yielding a quasi-planar surface. Optical devices were processed in the epi-islands using conventional fabrication processes. Source/drain n-type ion implants with standard ohmic contacts at the bottom of the DGWs and top-side p-type ohmic metal provided terminal access to the optical devices. The OEICs were completed by metallizing the top optical device contact to upper level metal pads connected to the electronics. Fully functional OEICs were optically and electrically characterized.
In conjunction with collaborators, numerous optical devices were demonstrated to be compatible with E-o-E fabrication. High-speed metal-semiconductor-metal (MSM) and high-gain optical-enhancement FET (OPFET) detectors were designed, fabricated in the commercial MESFET process and characterized. (In,Al,Ga)As LEDs, in-plane laser diodes, in-plane surface-emitting laser (IPSEL) diodes and multiple quantum well modulators/detectors were designed, MBE grown at E-o-E compatible temperatures, processed and characterized. (In,Ga)AsP LEDs and laser diodes were evaluated and determined to be optimal for E-o-E integration.

Nine E-o-E based OEIC chips were designed, fabricated and characterized in association with several collaborators. Among the OEICs demonstrated with these chips were analog neural-inspired threshold circuits with LEDs and OPFETs, analog neural-inspired winner-take-all circuits with LEDs and OPFETs, and digital transmit/receive high-speed circuits with MSMs, LEDs and IPSELs. A multi-epitaxial chip, with over fifty OEICs to develop five different optical devices, and an “optical bond pad” chip to develop drop-in cells for optical interconnects, were also designed. A multi-project chip termed OPTOCHIP, whereby several research groups jointly fabricate E-o-E based OEICs, is scheduled and represents the evolution of this work.

Thesis Supervisor: Clifton G. Fonstad, Jr.
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Chapter 1

Introduction

A serious performance limitation within present communication and computation systems is their inability to transfer large quantities of information at high rates. This information can be encoded as either electrical or optical signals and can be transmitted over either electrical or optical lines, called interconnects. Traditionally, integrated electronic circuits and electrical interconnects have adequately provided the necessary information transmission capacity. With the enormous advances in VLSI technology and digital systems in the past two decades, however, electrical interconnects are now being overwhelmed. Electrical interconnect limitations arise from the finite resistivity, capacitance and length of the electrical interconnect conductors. Electrical interconnect limitations were first felt in long-haul communications systems. A solution was sought and optics provided the answer. By transmitting optical signals through optical fibers, a tremendous gain in information capacity was achieved.

As data rates have continued to increase, electrical interconnects are now restricting the information transmission capacity at distances less than one millimeter, a length typical of the spacing between chips on a printed circuit board. Can optics once again provide the solution? The answer is potentially yes. Optical interconnections in principle offer solutions to several of these limitations as well as offer new interconnection architectures [1]. What remains to be answered is how to implement
the solution.

Unlike long-distance communication links where a single optical fiber, a discrete laser and separate drive electronics are well suited, optics will be successful at small size scales only if the optical interconnect, the optical emitter and detector, and the drive electronics can be constructed together. A new technology must be developed to elegantly intermix both optical and electrical devices at the size scale of state of the art electronics, namely very large scale integrated (VLSI) circuits. Necessary optical devices include semiconductor lasers, light-emitting diodes (LEDs), metal-semiconductor-metal (MSM) optical detectors, multiple quantum well (MQW) optical modulators and optical waveguides. Desired electrical devices include transistors forming a complete logic family, for example silicon p- and n-channel metal-oxide semiconductor field effect transistors (MOSFETs) forming the complementary-MOS (CMOS) family or gallium arsenide enhancement- and depletion-channel metal-semiconductor field effect transistors (MESFETs) forming the direct-coupled FET logic (DCFL) family.

Beginning in the early 1980’s, researchers proposed numerous technologies to allow optics and electronics to co-exist. These integration schemes fall into one of two categories, either hybrid, where the optics and the electronics are formed separately but are then packaged in close proximity, or monolithic, where the the optics and electronics are inherently proximal. In the case of semiconductor-optics and -electronics integration, which is considered exclusively in this work, monolithic means that that there is a common semiconductor crystal substrate. Whether the integration is hybrid or monolithic the goal is to take advantage of the inherent properties of the optics (i.e. communication interconnects) and to simultaneously take advantage of the inherent properties of the electronics (i.e. computation elements). In the case of hybrid integration the final assembly is called a hybrid optoelectronic component and in the case of a monolithic integration the term optoelectronic circuit (OEIC) applies. OEICs promise to yield higher system performance and are, therefore, the
category of interest in this work.

Several OEIC fabrication techniques have been successful in the past decade, but only for limited classes of communication and computation systems. The requirements placed on the integration technology are as varied as the final systems themselves. Poor manufacturability has riddled several integration techniques as has the premise that to produce optoelectronic circuits the electronic circuits themselves must be specially produced. Primarily for these reasons, we have proposed a novel optoelectronic integration technique aimed at providing a manufacturable method to integrate a wide variety of optical and electrical devices which has, as its starting point, state of the art commercially fabricated VLSI electronic circuits. This optoelectronic integration technique is termed Epitaxy-on-Electronics (E-o-E) and will be detailed in this thesis.

The remainder of this thesis is organized in the following manner. Chapter 1 briefly discusses the advantages of optical interconnects and overviews the various existing optoelectronic integration techniques. This overview provides a context for Chapter 2 which details the Epi-on-Electronics optoelectronic integration technique. Optoelectronic circuit design, electronic circuit fabrication, lowered-temperature molecular beam epitaxy (MBE), epitaxial "island" processing and optoelectronic circuit characterization are discussed in this chapter. A library of demonstrated and proposed optoelectronic devices compatible with the E-o-E technique is presented in Chapter 3. The thermal characterization of the commercial electronics begins the chapter, followed by various optical detectors, optical emitters and finally optical modulators which includes waveguides. This chapter emphasizes both the leverage which building on a commercial electronics base affords this integration technique as well as the flexibility which the E-o-E technique offers by being able to integrate a wide variety of optoelectronic devices. Chapter 4 presents various optoelectronic circuits, fabricated using the E-o-E technique, which serve as demonstration chips. Each subsection represents one physical chip which may have several different circuit designs in different
areas. This idea, that a single chip may have subregions with circuits specific to a particular optical device, leads naturally to the multi-epitaxy chip designed within the ARPA National Center for Integrated Photonics Technology (NCIPT) consortium for which MIT serves as the optoelectronic circuit design and OEIC project coordination center. This design (MIT-OEIC-3/NCIPT-OEVLSI-1) is detailed at the end of Chapter 4. Finally, Chapter 5 offers an assessment of where the E-o-E technology is currently positioned and how it may be further developed to become a fully manufacturable technology. A multi-project optoelectronic chip, termed OPTOCHIP, which is to be open to a wide user base is outlined as the logical precursor to an optoelectronic circuit foundry service. Conceptually this leads to a natural extension of the electronic circuit ARPA/NSF MOSIS service to form an optoelectronic circuit ARPA/NSF MOSIS - university service.

1.1 Advantages of Optical Interconnects

As suggested in the introductory remarks, optical interconnects offer several advantages as compared to electrical interconnects. These advantages become vital for high-density, high-speed interconnections typically required in modern communication and computation systems. Among these advantages are the following [1, 2, 3]:

1. Optical interconnects are immune to mutual coupling. This reduces noise and cross talk which are particularly detrimental in high interconnection-density parallel interconnects and cross-over circuits. High electromagnetic pulse (EMP) immunity means that optical interconnects are inherently radiation resistant.

2. Optical interconnects have reduced capacitive loading. This, and a signal return path not being required, reduce the number of interconnect paths and increase the maximum fan out.
3. Optical interconnects do not require a transmission media. This facilitates free-space interconnects and dynamically steered, with holograms or mirrors, interconnects.

4. Optical interconnects require less drive power. Drive power is lower for frequencies at which electrical interconnects require impedance matching.

5. Optical interconnects have high bandwidth. This is desirable for microwave and millimeter wave systems as well as for time and wavelength division multiplexing in digital systems.

To help visualize the various optical interconnect possibilities suggested in the items above, schematic representations of various optical interconnect types are shown in Figure 1.1. In the illustrations, chips are shown interconnected but are intended to represent any combination of cabinet, board or chip interconnections. The chips are generic (silicon, GaAs, or InP) and contain optical sources (laser diodes, LEDs or optical modulators) and detectors (MSM or p-i-n). The optical components can be either discrete devices, electrically connected in a hybrid fashion by various techniques such as bump-bonding, or monolithically integrated. Figure 1.1(a) illustrates a low-loss, commercially available optical fiber guiding the optical signal from chip-to-chip, (b) shows a monolithically integrated waveguide, formed by interdiffusion or dielectric patterning, connecting chips, (c) depicts a chip broadcasting an optical signal through free space to a holographic element which reflects the signal to all areas of another chip and (d) shows an optical signal transmitted from optoelectronic-computing plane to optoelectronic-computing plane, being received, processed, and retransmitted at each plane. Figures 1.1 (a) and (b) are representative of the category of optical interconnect termed "in-plane" conveying that the interconnect signal propagation direction is in the plane of the chip. Figure 1.1 (c) and (d), in contrast, are representative of the category of optical interconnect termed "surface-normal" simply meaning that the interconnect signal propagation direction has a significant directional component.
normal to the surface of the chip. Both classes of optical interconnect are useful and an integration technique should be capable of producing both categories.

Returning to the list of advantages of optical interconnects (OI’s), each will be briefly discussed by comparing the inherent properties of OI’s with electrical interconnects (EI’s).

1. **Immunity to mutual coupling.** Conventional EI’s suffer from mutual electromagnetic coupling effects. These effects become more severe as the signal bandwidth increases since the mutual coupling is proportional to the signal frequency. Unlike moving electrons, photons do not generate stray electric and magnetic fields. With proper design optical scattering can be minimized and, therefore, OI’s potentially offer communications channels with extremely low cross talk. For similar reasons, OI’s are insensitive to electromagnetic noise sources including EMPs.

2. **Reduced capacitive loading.** EI’s have an inherent capacitance which is proportional to the length and width of the interconnect. A signal in an EI must supply enough electrons to charge all attached load devices and the interconnect capacitance to the desired signal voltage. The associated RC time delays can be significant, which limits the available bandwidth. RC contributions come from both geometric layout determined line characteristics and from manufacturing process variations. The latter results in significant and unpredictable signal skew between load devices which is detrimental at high speeds [4, 5]. An optical signal on an OI must supply enough photons to charge only the attached load devices. There is no line-charging phenomenon present in an OI. Signal skew on OI lines is purely length dependent, is entirely predictable without complex electromagnetic modeling software and is less susceptible to manufacturing variations. There is, however, the equivalent to a resistive loss which results from optical absorption or scattering in the OI, or if the sources or detectors have less than perfect quantum efficiency.

3. **No medium required.** There are three significant consequences of the fact that OI’s do not require a transmission medium. First, EI’s must reside near a ground
Figure 1.1: Schematic representation of four optical interconnect realizations: (a) optical fibers, (b) integrated optical waveguides, (c) free-space reflection, (d) free-space transmission. Modified version of a figure in reference [2].
plane to assure that stray electric fields are properly terminated. OI's have no such constraint and, therefore, need not reside in the plane of the chip. OIs in all three dimensions are possible and numerous new interconnect architectures are possible. Free space plane-to-plane interconnection is one example. Second, EI's must avoid direct crossing and are instead routed over and under one another with interlevel dielectrics providing electrical isolation. OI's can be routed through one another without significant cross-coupling, provided that the angle of intersection is in excess of approximately 10° [1]. Finally, EI's also require mechanical contacts to conduct electrons while OI's do not require a physical conduit to transport photons. Thus, OI rerouting can be accomplished by changing the direction of the optical beams. Dynamic rerouting is particularly well suited for processing operations that entail global interconnections between elements of the input array, such as fast Fourier transforms and sorting.

4. Reduced drive power. EI drive power is proportional to the load capacitance, the operating frequency, and the square of the voltage swing. For very long interconnect distances, building-to-building or machine-to-machine for example, it is clear that the load capacitances, which include the line capacitances, will be quite large and thus the drive power will also be sizable. For shorter interconnect distances, gate-to-gate for example, the line capacitances are of the order of tens of femtofarads and the associated drive power is on the order of hundreds of microwatts, assuming 0 V and 3.0 V low and high signals, respectively, and 1 ns edges. For chip-to-chip interconnects the capacitance is of the order of hundreds of femtofarads, due to bonding pad capacitances, and the drive power is of the order of one milliwatt. If the frequencies are high enough that impedance matching is necessary, a loss term, $V^2/Z_o$, must be added to the drive power expression. Drive powers of hundreds of milliwatts are typical for terminated electrical lines. These trends are shown in Table 1.1.

OI drive power is also proportional to the load capacitance and frequency, but is linearly proportional to the voltage swing and inversely proportional to the detector
### 1.1. ADVANTAGES OF OPTICAL INTERCONNECTS

<table>
<thead>
<tr>
<th></th>
<th>Electrical</th>
<th>Optical</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gate-to-Gate</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance (C)</td>
<td>$2C_{gate} + C_{line}$</td>
<td>$2C_{gate} + C_{det.}$</td>
</tr>
<tr>
<td>Power</td>
<td>$\frac{CV^2}{2\tau}$</td>
<td>$\frac{CV}{\tau \eta_s (det.,resp.) + (IV_{laser})_{th}}$</td>
</tr>
<tr>
<td>Estimate</td>
<td>$0.33 \text{ mW}$</td>
<td>$1.9 \text{ mW}$</td>
</tr>
<tr>
<td><strong>Chip-to-Chip</strong></td>
<td></td>
<td></td>
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<tr>
<td><strong>Unterminated</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance (C)</td>
<td>$2C_{gate} + C_{line} + 2C_{pad}$</td>
<td>$2C_{gate} + C_{det.}$</td>
</tr>
<tr>
<td>Power</td>
<td>$\frac{CV^2}{2\tau}$</td>
<td>$\frac{CV}{\tau \eta_s (det.,resp.) + (IV_{laser})_{th}}$</td>
</tr>
<tr>
<td>Estimate</td>
<td>$1.6 \text{ mW}$</td>
<td>$1.9 \text{ mW}$</td>
</tr>
<tr>
<td><strong>Chip-to-Chip</strong></td>
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<td></td>
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<tr>
<td><strong>Terminated</strong></td>
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<tr>
<td>Capacitance (C)</td>
<td>$2C_{gate} + C_{line} + 2C_{pad}$</td>
<td>$2C_{gate} + C_{det.}$</td>
</tr>
<tr>
<td>Impedance ($Z_o$)</td>
<td>$\sqrt{\frac{L}{C}}$</td>
<td>$-$</td>
</tr>
<tr>
<td>Power</td>
<td>$\frac{CV^2}{2\tau} + \frac{V^2}{Z_o}$</td>
<td>$\frac{CV}{\tau \eta_s (det.,resp.) + (IV_{laser})_{th}}$</td>
</tr>
<tr>
<td>Estimate</td>
<td>$181.6 \text{ mW}$</td>
<td>$1.9 \text{ mW}$</td>
</tr>
<tr>
<td><strong>Board-to-Board</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Terminated</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance (C)</td>
<td>$2C_{gate} + C_{line} + 2C_{pad}$</td>
<td>$2C_{gate} + C_{det.}$</td>
</tr>
<tr>
<td>Impedance ($Z_o$)</td>
<td>$\sqrt{\frac{L}{C}}$</td>
<td>$-$</td>
</tr>
<tr>
<td>Power</td>
<td>$\frac{CV^2}{2\tau} + \frac{V^2}{Z_o}$</td>
<td>$\frac{CV}{\tau \eta_s (det.,resp.) + (IV_{laser})_{th}}$</td>
</tr>
<tr>
<td>Estimate</td>
<td>$183.4 \text{ mW}$</td>
<td>$1.9 \text{ mW}$</td>
</tr>
</tbody>
</table>

$^1 C_{gate} = 1.7 \text{ fF} \ (\text{length} = 0.5 \mu\text{m}, \text{width} = 1.0 \mu\text{m}, t_{ox} = 10\text{nm}, \epsilon_{ox} = 3.9), C_{line} = 69 \text{ fF} \ (\text{length} = 1\text{mm}), V = 3.0 \text{ V}, \tau = 1\text{ns}$

$^2 C_{det.} = 33 \text{ fF} \ (t = 2\mu\text{m}, A = 625 \mu\text{m}^2), \text{det.\,resp.} = 0.5 \text{ A/W}, \eta_s = 25\%, (IV_{laser})_{th} = 1 \text{ mW}$

$^3 C_{pad} = 173 \text{ fF} \ (A = 100 \mu\text{m}^2), C_{line} = 4 \text{ fF} \ (\text{length} = 1 \text{cm}, \text{width} = 25 \mu\text{m}, t = 500 \mu\text{m})$

$^4 Z_o = 50 \text{ \Omega}$

$^5 C_{line} = 400 \text{ fF} \ (\text{length} = 1 \text{m}, \text{width} = 25 \mu\text{m}, t = 500 \mu\text{m})$

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Table 1.1: Interconnect power comparison. EI's consume less power for short distances and/or slow speeds while OI's consume less power for long distances and/or high speeds. Modified analysis found in reference[2].
responsivity and quantum efficiency. In addition, any power required to reach optical threshold must be included. With typical laser threshold voltages of roughly one volt and threshold currents of approximately 1 milliampere (though threshold currents continue to drop), optical interconnect drive powers always exceed 1 milliwatt. The use of LEDs, which have no threshold current, will not suffer from this drive power floor, which may be useful if operating speeds do not require laser diodes [6]. Since OI's do not have associated line capacitances, the drive power will stay relatively constant as the interconnect distance is increased. Thus it is clear that OIs require lower drive power for very long distances, but a higher drive power for extremely short interconnect distances than the EI counterpart. Table 1.1 compares the gate-to-gate, chip-to-chip unterminated, chip-to-chip terminated and board-to-board drive powers for electrical and laser-driven optical interconnects using typical device values. Table 1.1 suggests that laser-driven OIs are advantageous for board-to-board interconnects and chip-to-chip interconnects at frequencies requiring load impedance matching as well as for longer-haul interconnects.

5. **High bandwidth.** The previous four OI advantages suggest that OIs promise superior performance by offering reduced channel cross talk, increased fan out and lower power operation in a host of traditional and new interconnect architectures. OIs also offer extremely high bandwidth operation due to the high carrier frequency ($\sim 10^{14}$ Hz). This bandwidth is for a single channel. However, the ability to operate hundreds of OI channels in parallel, all at high speeds and in close proximity, without interference effects is perhaps the true glory of OIs. It is this parallel nature which must be exploited to reach extremely high information throughputs.

Figure 1.2 shows the distribution of optical interconnects, electrical interconnects and optical telecommunication systems in frequency-distance space. The interconnect distance is plotted on the horizontal axis while the achievable communication bit rate per channel is plotted on the vertical axis. While exact performance estimates of the various technologies are difficult to calculate, a composite plot such as this is useful
Figure 1.2: Distribution of optical interconnects, electrical interconnects and optical telecommunication in the frequency-distance space. The shaded box represents the short distance, high throughput domain requiring large-scale, high-density, high-speed and low power monolithic optoelectronic circuits. Modified figure found in reference [3].
to demonstrate trends.

At the longest distances, single-mode optical fibers dominate and with the addition of optical fiber amplifiers these transmission lengths can be further extended. Optical trunk lines use single-mode fibers while optical local-area networks typically use multi-mode fibers. Though these fibers can be useful at distances much shorter than kilometers, the lengths shown are the most common. Low-loss co-axial electrical cables overlap with multi-mode fibers as well as fiber guided OIs. In this context a distinction is made between optical fibers, both single- and multi-mode, and OIs. Optical fibers are optically pumped by discrete lasers and drive electronics while the OIs are defined as having the optical emitter/detector integrated with the electronics. At shorter distances, typically one meter or less, waveguided and free space OIs are useful where electrical interconnects are traditionally used. In this context EIs refer to wire bundles driven by electronics. Below approximately ten centimeters the distances are comparable with printed circuit boards, while below about one centimeter distances are comparable with integrated circuit chips. Monolithic electrical interconnect lines, typically aluminum, route electrical signals at these distances. Below about 1 millimeter the distinction between devices and interconnects, both optical and electrical, becomes less clear because interconnect lengths are on the order of the device sizes. This is the domain of monolithic optoelectronic VLSI circuits. To produce very short electrical interconnections, interlevel interconnect wires are routinely used in integrated circuits. Short optical interconnects can be either free space or waveguided and must have an optical emitter/detector monolithically integrated with the drive electronics.

Shifting attention to the vertical axis, it is seen that all single-channel interconnect bit-rates are bounded from above by either the laser or modulator modulation limit. This limit can be exceeded by operating several channels in parallel. Wavelength division multiplexing (WDM) and parallel fibers denotes the idea that a fiber carrying multiple wavelengths signals or a bundle of fibers can extend the aggregate bit rate
1.2. MONOLITHIC OEIC FABRICATION APPROACHES

nearly indefinitely. The number of channels per unit cross-sectional area is an important figure of merit which is limited by the fiber optical cable cladding thickness. Superconducting wires can extend the bit rate of a single channel by reducing the resistance to zero, thereby eliminating RC time constants, though parallel lines will still interfere. Free space OIs, on the other hand, can have densely packed parallel channels while maintaining high speeds. Optoelectronic drive and receive circuits are the major limit on the bandwidth-channel density product, called information flux with units of Hz/cm². As shown in the shaded box at short distances, a large-scale, high-density, high-speed and low-power monolithic optoelectronic integrated circuit technology could drive optical signals into and receive optical signals from massively parallel OIs. Such an optoelectronic circuit technology is the goal of this thesis and the next section will overview the various approaches, including the one developed in this work.

1.2 Monolithic OEIC Fabrication Approaches

As briefly discussed in the introductory remarks, there are two general categories of optoelectronic integration, hybrid and monolithic. Hybrid integration brings together separately optimized optics and electronics through a variety of techniques such as wire and flip-chip bonding. Monolithic integration employs a common semiconductor substrate on which both optical and electrical devices are formed. Epitaxial lift-off, an integration technique whereby optical epitaxial layers are separated from a thick substrate and areoverlayed on electronic circuits, falls between hybrid and monolithic techniques. While hybrid integration offers good solutions for several applications, monolithic integration can lead to a reduction in cost, an increase in functionality and an improvement in performance over similar hybrid circuits [7]. There are several reasons for this. First, monolithic integration replaces hybrid integration bond wires, which have appreciable inductance, and flip-chip bump-bonding pads, which have
While E is not truly a monolithic approach, it is considered here.

<table>
<thead>
<tr>
<th>Approach</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
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</thead>
<tbody>
<tr>
<td>1. Structure</td>
<td>Common Epilayers</td>
<td>Electronic-Epi Above Photonic-Epi</td>
<td>Electronic-Epi Below Photonic-Epi</td>
<td>Epi-In-a-Well</td>
<td>Epitaxial Lift-Off</td>
<td>Photonic-Epi on Silicon VLSI ICs</td>
<td>Photonic-Epi on GaAs VLSI ICs</td>
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<td>2. Upper-level</td>
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<td>Added after growth</td>
<td>Added after growth</td>
<td>Added after growth</td>
<td>Commercially fabbed along with circuits</td>
<td>Added after growth</td>
<td>Commercially fabbed along with circuits</td>
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<td>Interconnection</td>
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<tr>
<td>3. Planarity</td>
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<td>Poor</td>
<td>Good</td>
<td>Good</td>
<td>Poor</td>
<td>Good</td>
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<td>4. Lithography</td>
<td>E-beam</td>
<td>Photo</td>
<td>E-beam</td>
<td>Photo</td>
<td>Photo</td>
<td>E-beam</td>
<td>Photo</td>
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<td>5. Electronic</td>
<td>Common epi restricted</td>
<td>Ion-MESFET, H-FET and HBT</td>
<td>Ion-MESFET and H-FET</td>
<td>Ion-MESFET</td>
<td>Bi-CMOS VLSI</td>
<td>Bi-CMOS VLSI</td>
<td>Ion-(E/D)MESFET VLSI</td>
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<td>7. IC Complexity</td>
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<tr>
<td>Now</td>
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<td>MSI</td>
<td>SSI</td>
<td>MSI</td>
<td>MSI</td>
<td>MSI</td>
<td>VLSI</td>
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<td>Future</td>
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<td>MSI</td>
<td>MSI</td>
<td>MSI</td>
<td>LSI</td>
<td>VLSI</td>
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<tr>
<td>8. Fabrication</td>
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<td>Moderate</td>
<td>High</td>
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<td>Low</td>
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<tr>
<td>Complexity</td>
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<tr>
<td>9. Development</td>
<td>Caltech</td>
<td>Hitachi</td>
<td>AT&amp;T</td>
<td>Honeywell</td>
<td>Georgia Tech</td>
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<td>MIT</td>
</tr>
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<td>Centers</td>
<td>Xerox</td>
<td>AT&amp;T</td>
<td></td>
<td>Fujitsu</td>
<td></td>
<td>MIT LL</td>
<td>with Caltech</td>
</tr>
</tbody>
</table>
significant capacitance, with lithographically defined metal lines. Stray electric and magnetic fields and cross talk are thereby reduced. Second, monolithic integration increases integration density. Numerous applications, particularly two-dimensional optical signal switching and processing, require high density arrays of optical emitters or modulators, detectors, and electronic logic. Hybrid integration requires mechanical “hunt and place” procedures which inherently limit the integration density even with sophisticated self-aligning structures and balled-metals. Functionality, therefore, increases with monolithic integration. Third, self-alignment of optical emitters and detectors is an automatic consequence of monolithic integration. Coupling losses are thus decreased. Finally, monolithically integrated optoelectronic circuits should have a higher yield, lower cost, and overall more manufacturable in cases where high integration density is required [7]. It appears that a growing number of optoelectronic applications can benefit from the advantages that monolithic integration offers. This is strong motivation to develop a robust monolithic integration technology.

Yariv’s group at Caltech is credited with reporting the first experimental OEIC study in 1978-1979 which involved the integration of an AlGaAs/GaAs laser with a Gunn diode [8] and with GaAs MESFETs [9] on GaAs substrates [10]. Since then, numerous monolithic optoelectronic integration techniques have been investigated. Taken together these techniques have firmly established the field of integrated optoelectronics even though each method contains inherent technological difficulties. After briefly overviewing several alternate monolithic fabrication approaches, the integration technique proposed and investigated in this thesis will be introduced. This technique will be detailed in Chapter 2.

Table 1.2 lists the key monolithic optoelectronic integration techniques including the method proposed in this work (column G). A fabrication cross section is given for each technique, as is a brief assessment of several fabrication issues. Upper-level interconnection refers to the metal lines that are required to interconnect the electronic devices. Techniques that build on a commercial electronics base can have
these lines fabricated along with the electronic circuits as opposed to adding these lines after epitaxial growth. The planarity of the final optoelectronic circuit is crucial since at least the final optical to electric device interconnection requires lithographical and metallization steps. Lithography is most readily performed by spinning photore sist and optically patterning features, both of which require nearly perfectly planar surfaces. Metal step coverage is difficult to achieve on a nonplanar surface and, therefore, also benefits from planarity. Lithography techniques such as e-beam writing and metallization methods such as sputtering must be employed in techniques with poor planarity. Since the type of optical and electrical devices required in a given optoelectronic circuit can be as varied as the optoelectronic system applications themselves, in general an integration technique should be able to intermix several different optical devices and electrical devices. The technique itself can impose fabrication constraints which limit this selection. It is also desirable to reach large-scale and high-density optoelectronic circuit levels, termed optoelectronic VLSI (OE-VLSI), with a minimum of fabrication complexity. The final row in Table 1.2 lists the major development centers for the various integration techniques.

**A. Common Epilayers.** This approach to monolithic optoelectronic integration is to fabricate both optical and electrical devices in the same epitaxial layers. For example, since HBT and laser diode heterostructures are similar, it seems reasonable to simply process selected areas of a wafer into HBTs and other areas into laser diodes. Numerous OEICs have been fabricated using this technique including lateral current injection (LCI) laser diodes with FETs [11], LCI laser diodes with lateral HBTs [12] and vertical HBTs with LEDs [6]. Unfortunately this approach does not allow for the independent optimization of both optical and electronic devices. Independent optimization is a serious issue since high performance optoelectronic systems require both state-of-the-art optical devices (e.g. lasers) and electrical devices (e.g. transistors). In addition, poor planarity and electronic device uniformity restrict this technique to small to medium scale integration.
1.2. **MONOLITHIC OEIC FABRICATION APPROACHES**

**B. Electronic Epitaxy Above Photonic Epitaxy.** This is one method which avoids compromising optical and electrical device performance by separating the optical and electrical device epitaxial heterostructures. By growing the optical device layers, which are typically quite thick (3-8 μm), beneath the electrical device layers, which are typically quite thin (≈ 1 μm), both set of layers can be independently optimized while maintaining reasonable planarity. This planarity is a result of only removing a thin layer of material (i.e. the electronic layers) to gain access to the thick layers (i.e. the optical layers) in the lateral areas where optical devices are to be formed. This technique is well suited to integrate a wide variety of optical and electrical devices while retaining the ability to use photolithographic processing. Double-diffused LCI lasers [11], linear electro-optic modulators, waveguides and enhancement/depletion (E/D) MESFETs [13] have been fabricated using this technique. There are two significant drawbacks to this approach, however. First, either the optical devices must be undoped or a doped shield layer must be grown between the optical and electrical layers. If the optical layers are doped and extend underneath the electrical layers the high-frequency performance of the electrical devices will be compromised due to backgating and cross-talk effects [14]. One solution to this is to incorporate a conducting shield layer just below the electrical device and hold this layer at a fixed potential (i.e. fix the backgate potential). Though this increases the processing complexity, such shield layers are routinely grown and contacted in the AT&T field-effect transistor - self-electrooptic device (FET-SEED) process with good success [15]. The second drawback to this technique is that the electronic devices do not take advantage of the considerable commercial electronics infrastructure. By fabricating all electronic devices, this technique must address the stringent uniformity requirements vital to large-scale integration. This is a serious problem and it remains to be seen if sufficient uniformity can be achieved for a set of devices forming a low-power logic family, for example DCFL. While there has been reasonable success with depletion-mode HFETs in the AT&T FET-SEED process, enhancement-mode
devices have not been fabricated.

C. Electronic Epitaxy Below Photonic Epitaxy. This integration approach is very similar to the electronic epitaxy above photonic epitaxy method just described, except that the electronic layers are grown below the photonic layers. This successfully avoids backgating problems by fabricating the electronic devices directly on the semi-insulating substrate. Predictably, however, etching through the thick layers to reach the electronic layers produces large steps (i.e. several microns) which makes subsequent processing much more difficult. Spun photoresist uniformity is compromised, lithography is restricted to long focal length techniques such as e-beam, and metal step coverage is more difficult. For these reasons this integration scheme has not been used for more than simple demonstration optoelectronic circuits.

D. Epitaxy-in-a-Well. A clever idea to circumvent the problem of poor planarity and backgating is to etch a well in selected areas of a semi-insulating substrate, grow the desired photonic heterostructure in just this well region and finally process photonic devices in the epitaxial region and electronic devices in the surrounding bulk substrate areas. This technique has been used to integrate LEDs with ion-implanted MESFET circuits [16]. There are still two serious drawbacks to this integration technique, however. First, to achieve high crystalline quality at the bottom of the well a crystallographic wet etch is used to form the well. If the top surface of the photonic devices is to be planar with the top of the non etched substrate, a well approximately 5 \( \mu \text{m} \) deep must be etched. This results in the loss of 5 \( \mu \text{m} \) of substrate around the perimeter of the well assuming a 45° V-groove etch profile. This introduces an area "overhead" which becomes significant for even moderately sized wells (e.g. 20 \( \mu \text{m} \times 20 \mu \text{m} \)), let alone smaller areas on the order of SEED windows or vertical-cavity surface-emitting lasers (VCSELs) which can reach 5 \( \mu \text{m} \times 5 \mu \text{m} \) or less. This sidewall profile issue ultimately limits the integration density. The second drawback, common to all integration techniques discussed thus far, is that the electronics must be formed from scratch. This method relies on ion-implanted devices such as MESFETs and does
not support epitaxial electronic devices without a regrowth step where the electronics would similarly be recessed in well$, which adds significant complexity to the process. Ion-implanted MESFETs are sufficient electronic devices for most optoelectronic circuit applications and are produced commercially (Vitesse Semiconductor Corp. and Motorola) with excellent uniformity. To reiterate, while restricting the electronic devices to ion-implanted MESFETs is not a serious issue, controlling the uniformity is a problem unless done commercially. It is doubtful that wafers with photonic epitaxy in wells could be run through a commercial GaAs ion-implantion MESFET process because of the high-temperature implantation anneals required (typically $800^\circ C$ for 1 hour). In addition, it is unclear whether optical devices could withstand the stresses caused by thick interlevel metallization and dielectric deposition essential to large scale integrated circuits.

E. Epitaxial Lift-Off (ELO). As previously mentioned, the epitaxial lift-off integration technique falls between hybrid and monolithic methods. ELO is discussed here both because there ultimately is a direct photonic-epitaxy to electronic-crystal contact as well as because of recent work which has established ELO as being competitive with monolithic integration in some areas. The ELO technique begins by growing the optical epitaxial layers on a bulk substrate. These layers are then coated in wax (Apiezon W wax [17]) and the substrate is etched away leaving only the epilayers embedded in the wax. This etching exploits the high selectivity of hydrofluoric acid (HF) in etching AlAs without etching GaAs. The epilayers are then floated (in de-ionized water) over to and aligned with electronic circuits with the single-crystal substrate exposed in selected areas. The circuits can be either silicon or GaAs. The thin-film layers are then gently pushed against the electronic substrate, the water is dried and the layer is held in place by short-range attractive van der Waals forces [18, 19]. The wax is then removed and final optical to electrical device interconnection is formed if a fully fabricated optical device was fabricated prior to lift-off; otherwise, full photonic device processing is conducted [20].
CHAPTER 1. INTRODUCTION

This technique has several attractive features. First, the optical and electrical devices can be optimized completely independently. Photonic devices may be grown in a variety of material systems under nearly any conditions. Second, the electronic devices can be either silicon or III-V based. Third, in the case of silicon VLSI CMOS circuits and ion-implanted VLSI GaAs MESFET circuits, commercial foundries may be used. Finally, in addition to taking full advantage of industrial electronic circuit manufacturing for the intrinsic devices, all upper-level interconnect metallization can also be used. This is an extremely important advantage which all of the previously discussed integration techniques do not share. In fact, it is the advanced fabrication of these upper-level interconnects which give VLSI circuits their high densities and high performance. In other words, even if the previously discussed techniques could fabricate highly uniform electronic devices that is only half of the battle. The optical devices would also need to be able to withstand the formation of up to $\sim 4 \ \mu\text{m}$ of interlevel dielectric and up to 4 levels of interconnect metals. This is exceptionally difficult to achieve even with perfectly planar devices because the interconnects themselves introduce nonplanarity. Once again, the ELO technique can take advantage of fully processed circuitry.

There are a few unanswered questions with this method which may be considered drawbacks. First, it remains to be seen if ELO optoelectronic circuit reliability can reach the levels of truly monolithic optoelectronic circuits. This is a question of interface quality, thermal dissipation from the optical devices and mechanical ruggedness. A second question is how large and how dense can arrays of these devices be fabricated. Large arrays on thin films may become distorted, which sets a size limit. The alignment process may also bound the maximum density. The ELO structure shown in Table 1.2 depicts a bottom side contact. If the interface is not of sufficient quality to conduct current without a large voltage drop, two top-side contacts to the optical devices would be necessary, which would reduce the achievable integration density. Finally, manufacturability is a concern when handling thin films that must
be precisely aligned. These questions will be answered with time; for now it appears to be a promising integration technique for at least medium-scale integrations.

F. Photonic Epitaxy on Silicon VLSI ICs. From the discussion of the previous five techniques it is apparent that planarity, independent device optimization and high integration density are all important criteria for assessing a particular integration approach. However, perhaps an even more important criterion, as indicated in the epitaxial lift-off discussion, is the ability an integration technique has to leverage the enormous commercial silicon or GaAs VLSI circuit industries. Commercial foundries offer state-of-the-art circuits with excellent electronic device uniformity as well as a full complement of multilevel interconnect metalizations. Monolithically building on this base is the approach taken by the final two integration techniques shown in Table 1.2, namely photonic epitaxy on silicon VLSI ICs and photonic epitaxy on GaAs VLSI ICs.

The objective of the photonic epitaxy on silicon VLSI ICs method is to epitaxially grow, either selectively or subtractively, GaAs/AlGaAs heterostructures in oxide openings on either partially or fully processed silicon circuits. This would leave photonic epitaxial “islands” intermixed with the electronic devices, and interconnection of these devices would yield optoelectronic circuits. Up to now it has been implicitly assumed that active emitters are the optical devices for which an integration technology should be evaluated. This deserves qualification. Optical emitters can only be fabricated from direct band gap materials (e.g. (In,Al,Ga)AsP) and silicon is an indirect band gap semiconductor. Indirect band gap materials do serve well as detectors and silicon p-i-n diodes and photosensitive BJTs are in widespread use. Optical modulators require direct band gap materials. For these reasons, an integration technology flexible enough to incorporate optical emitters and modulators require direct band gap material, for example, GaAs/AlGaAs. This is the motivation for growing GaAs/AlGaAs heterostructures, on a silicon substrate in this case.

The overwhelming drawback with this approach is the material incompatibility
between the silicon substrate and the GaAs/AlGaAs epitaxial layers. There are large differences in lattice constants (Si, 5.431 Å; GaAs, 5.654 Å; and AlAs, 5.654 Å) which leads to high defect densities at the interface and into the grown GaAs/AlGaAs. These dislocations compromise the GaAs/AlGaAs layer quality and adversely affect the devices fabricated in the material, especially high minority carrier current devices such as LEDs and lasers. A 1-2 μm GaAs buffer and strained layer superlattices can be used to trap some of these defects, but even then only optical modulators have been fabricated with any real success [21] although laser diodes have been demonstrated [22]. In addition to the lattice mismatch, there is also a thermal expansion mismatch between the materials and means that the III-V epilayers are severely strained (tensilely). Long term reliability is a major concern. In addition to these fundamental problems, there is also an important technological drawback to this technique. Ohmic contacts in silicon circuits are routinely formed with Al/Si or Al/Si/Cu to n- or p-doped silicon contact regions. At typical GaAs/AlGaAs growth and annealing temperatures (550º-700ºC) there are adverse interactions at this contact which degrades ohmic contact resistances. Therefore the ohmic contact and upper-level interconnect metallization must be added after the photonic epitaxy is grown. This integration can not take full advantage of the commercial circuits.

G. Photonic Epitaxy on GaAs VLSI ICs — Epitaxy-on-Electronics (E-o-E). From the discussion in the previous section, photonic epitaxy on silicon VLSI ICs, it is clear that an integration technique that is to take full advantage of commercial VLSI circuits must be capable of growing lattice matched optical devices on fully processed electronic circuits. The Photonic Epitaxy on GaAs VLSI ICs integration technology does just that. By growing GaAs/AlGaAs optical epitaxial layers on a commercial VLSI GaAs ion-implanted E/D MESFET circuit base, lattice matched devices are guaranteed because the circuit substrate is GaAs. Because ohmic contacts and Schottky barrier gates to GaAs are best formed from refractory metals, which do not react with GaAs even at temperatures above 600ºC, GaAs heterostruc-
tures can be grown on fully processed circuits containing tungsten-based gate metal, nickel-based ohmic metal and aluminum-based interconnect metals. This integration technique was first proposed by K.V. Shenoy and C.G. Fonstad, Jr. at MIT in 1992 [23] as the result of encouraging preliminary refractory-metal VLSI GaAs MESFET thermal studies [24]. This technique has been termed Epitaxy-on-Electronics (E-o-E) and is a novel solution to all of the drawbacks inherent in the other integration methods. It should be stated, however, that it is doubtful that a single optoelectronic integration technique can be flexible enough to meet all present and future systems demands. It is also the case that all fabrication flows have constraints which may be more or less restrictive depending on the particular devices to be integrated and the particular system specifications to be met. The dominant constraint in the E-o-E integration technique is that the photonic epitaxy must be grown at a temperature of 470°C or less. This does not, however, restrict the variety or performance of optical devices that may be grown on VLSI GaAs MESFET circuits. It simply means that lowered-temperature growth techniques, which have been developed in the past five years, must be employed. An additional issue is the area, in addition to the area of the optical device, which must be allocated to allow for a single-crystalline to polycrystalline material transition region. A 5 μm transition length is typical, though possibilities exist to reduce this dimension.

Understanding the physical constraints of this technique and demonstrating its capabilities has been the goal of this work and is the theme of this thesis. Chapter 2 provides a detailed description of the E-o-E technique and its constraints. Subsequent chapters demonstrate its capabilities and the final chapter projects its future possibilities.
Chapter 2

Epitaxy-on-Electronics Integration Technique

From the discussion in Chapter 1, it is evident that a robust and flexible monolithic optoelectronic integration technique is in demand to produce optoelectronic circuits for optical interconnect applications. Unfortunately, existing integration techniques (Table 1.2 columns A-F) are limited and a new approach to monolithically intermixing optical and electrical devices is paramount. To address this demand, we have proposed and demonstrated a novel optoelectronic integration technique (Table 1.2, column G) which promises to solve many of the shortcomings of the existing methods. This new technique, termed Epitaxy-on-Electronics (E-o-E), fully leverages the existing commercial VLSI GaAs MESFET electronics industry and thereby benefits from its considerable development. The E-o-E technique produces VLSI density optoelectronic circuits in four steps: design of electronic circuits with selected areas reserved for optical devices, commercial foundry fabrication of the electronic circuits, epitaxial growth of optical devices in the reserved areas and, finally, optical device fabrication and interconnection with the electronic circuitry.

This chapter serves as a detailed description of the E-o-E integration technique, its capabilities and its constraints. Figure 2.1 is a flow chart of the E-o-E pro-
cess. Each step (oval) will be briefly overviewed in the first section, Section 2.1. The remaining sections elaborate on the following steps: optoelectronic circuit design (Section 2.2), electronic circuit fabrication (Section 2.3), dielectric growth well preparation (Section 2.4), lowered-temperature molecular beam epitaxy (Section 2.5), epitaxial "island" processing (Section 2.6) and optoelectronic circuit characterization (Section 2.7).

2.1 E-o-E Integration Overview

To produce large-scale, high-density monolithic optoelectronic integrated circuits (OE-VLSI) it is advantageous to begin with a mature, commercial VLSI electronics technology. Until a few years ago silicon-based VLSI CMOS was the only choice. In the mid to late 1980's, however, Vitesse Semiconductor Corporation, based in Camarillo, California, began to commercially produce VLSI GaAs E/D MESFET circuits, primarily for high-speed digital circuits [25]. Of particular interest, Vitesse serves as the GaAs circuit vendor for the ARPA/NSF MOS Implementation System (MOSIS) [26], based in Marina del Rey, California, and associated with the University of Southern California, which is the Si and GaAs circuit broker for U.S. university projects. GaAs circuit fabrication is particularly accessible through the MOSIS/Vitesse pairing.

There are three keys to Vitesse's success in manufacturing GaAs E/D MESFET circuitry. First, they developed a proprietary process to multiply implant 4-inch-diameter semi-insulating GaAs wafers. This implant sequence is performed before device fabrication begins and ultimately leads to excellent transistor threshold voltage uniformity that is essential for VLSI circuits. Second, refractory-metal-based gate and ohmic contacts are used instead of gold-based metals to increase device lifetime and high-temperature operation. These low-reactivity refractory-metals, which can withstand extended time-temperature cycles, are the enabling technology for the E-
Figure 2.1: Optoelectronic circuit fabrication flow using the E-o-E integration technique (read top to bottom). The dashed line and arrow indicates that selective dielectric removal, to form dielectric growth windows (DGWs), is largely done at Vitesse.
o-E integration technique (i.e. the gate and ohmic contacts can withstand epitaxial
growth time-temperature conditions). Finally, all back-end processing such as inter-
connect metallization and interlevel dielectric planarization is identical to silicon
VLSI processes. These three advances uniquely positioned Vitesse in the VLSI GaAs
MESFET market for several years. Only recently have they been joined by Motorola.
The Vitesse VLSI GaAs MESFET fabrication process will be discussed further in
Section 2.3 and the time-temperature stability of the circuits will be detailed in Sec-
tion 3.1.

With the existence of commercially available VLSI GaAs E/D MESFET circuits
came the possibility of using these integrated electronic circuits as the starting point
for an optoelectronic circuit technology. The most straightforward approach would
be to start with fully fabricated electronic circuits and etch through the interlevel
dielectric stack to expose the underlying GaAs substrate (such etches are further
discussed in Sections 2.3 and 2.4). These areas, termed dielectric growth windows
(DGWs), could then serve as the seed crystal for lattice matched crystal growth. If a
growth technique such as metal-organic chemical vapor deposition (MOCVD) is used,
then conditions can be found in which single-crystal material will grow only in the
DGWs and no material will deposit in the inter-DGW region. This inter-DGW re-
region comprises the top overglass layer and bond pads, both from the standard Vitesse
process. Such selective grow is ideal, but not essential. If a growth technique such as
solid-source molecular beam epitaxy (MBE) or gas-source MBE is used, then single-
crystal material will grow in the DGWs and polycrystalline material will deposit in
the inter-DGW regions. The polycrystalline material can be stripped away in several
ways including wet chemical etch, dry etch and polishing. The essential feature of
any of these growth methods is that the total thickness of the optical device het-
erostructures grown in the DGWs can be precisely controlled and ideally is aligned
with the top of the surrounding dielectric side wall (DSW). This DSW is the edge of
the inter-DGW region. The top of the DSW and the top layer of the inter-DGW are
one and the same. The result of this epitaxial growth on fully processed electronic circuits is that epitaxial "islands" (epi-islands) are formed in the DGWs. After any deposited polycrystalline material is removed from the inter-DGW regions, the circuit is once again planar which is essential for high-resolution photolithography. The E-o-E technique takes full advantage of commercial VLSI electronics and back-end processing. Unlike similar integration techniques using silicon circuitry (Table 1.2, column F), the optical devices are lattice matched to the substrate and have identical thermal expansion coefficients. These advantages are critical to epitaxial layer quality and device lifetime.

At this point in the E-o-E process, there are conceivably hundreds or thousands of epi-islands where the DGWs once were. The top surface is planar, within some tolerance, and the epitaxy needs to be processed into functional optical devices such as LEDs, laser diodes or SEEDs. Once again, the straightforward approach is to treat these electronic circuits with planar epi-islands as a bulk substrate and process it as nonintegrated optical devices are processed. Optical devices require wet chemical etches, dry etches, dielectric depositions, metalizations, rapid thermal anneals and high-resolution photolithography (<1.0 μm critical dimension, <0.5 μm alignment tolerance). The thermally stable electronic circuits and the mechanically rugged epi-islands can withstand all of these processes. These processing steps not only form the intrinsic optical device, but they also connect the optical devices with the electrical devices. A bottom-side, n-type contact to the optical device can be implicitly formed if the DGWs are implanted with a source/drain implant and contacted at the edge with an ohmic contact. This can be achieved with standard steps in the Vitesse process. The top-side, typically p-type contact to the optical device can be made at the same time that a metal line is formed over to a nearby bond pad. This bond pad, which can be significantly smaller than a bond pad for wire bonding (e.g. 5 μm × 5 μm instead of 100 μm × 100 μm), is connected to an electrical device with standard interconnect levels. Thus optical and electrical device interconnection is
CHAPTER 2. EPITAXY-ON-ELECTRONICS INTEGRATION TECHNIQUE

photolithographically defined, resulting in minimal parasitic effects. The epi-islands process is elaborated upon in Section 2.6.

The optoelectronic circuits chip is now complete. The chip has standard electrical bond pads (100 \( \mu \text{m} \times 100 \ \mu \text{m} \)) to access the electronic circuits, for example, bias rails and input/output pads. Standard bond pads are also present to bias the optical devices. Optical input and output to the optical devices is achieved either by surface-normal or in-plane beams. Both optical device configurations are supported in the E-o-E process. All interconnection between the optical and electrical devices is also present and the chip is ready for optoelectronic characterization. This is further described in Section 2.7.

Figure 2.2, read clockwise from upper left, shows the E-o-E design and fabrication flow. Optoelectronic circuits are designed using standard Vitesse design and layout rules. These designs can be collected from a variety of groups and merged onto a single chip. All designs on this single chip ideally require the same optical heterostructure, though since several chips are produced from a single MOSIS/Vitesse fabrication run, different heterostructures can be grown on different chips. This results in only certain designs on a given chip, with a particular heterostructure grown on that chip, having full optoelectronic functionality. Chips with designs that all require the same heterostructure to be grown are termed "multi-project" chips while chips with designs that require a variety of different heterostructures to be grown are termed "multi-epitaxy" chips. After the designs are merged, the design is electronically transferred to MOSIS where it is placed in the reticle with other designs from other universities. These other designs can also be optoelectronic, though they are typically standard electronics-only designs. If available, blank space is left around the OEIC design. This space is left attached to the OEIC design when the chips are sawed and will eventually accommodate photoresist edge buildup temporarily present during optical device fabrication. The design is then sent to Vitesse, via a mask house, where the electronic circuit portion of the OEIC is fabricated. Two reactive-ion etch layers,
Figure 2.2: Schematic illustration of the Epitaxy-on-Electronics (E-o-E) design and fabrication flow (read clockwise starting from upper left). OEIC designs are combined at MIT and (a) the VLSI GaAs circuits are fabricated at Vitesse Semiconductor Corp. via the MOSIS service. (b) Heterostructures (e.g. LEDs) are epitaxially grown in dielectric growth windows (DGWs), which expose the underlying GaAs substrate, and (c) the resulting epi-islands are processed into functional devices. Finally, the optical and electrical devices are monolithically interconnected and the chips are disseminated.
Figure 2.3: Artist’s perspective of three stages of E-o-E optoelectronic circuit fabrication: (a) custom designed chip with dielectric growth window(s) as received from the foundry, (b) single-crystal material grown in the dielectric growth window and polycrystalline material deposited on the top overglass and bond pads, (c) planarizing polycrystalline etch, device definition and optical to electrical device interconnection which completes the fabrication sequence. The LED serves as a representative heterostructure.
which are part of the standard Vitesse process, specify the DGWs. This cuts through
the dielectric stack, in the DGW areas, to within roughly 1 μm of the underlying GaAs
crystal. The chips are sawed apart and returned to MIT where the chips are masked
and the final ~ 1 μm of dielectric material in the DGWs is wet etched away, leaving a
growth-ready GaAs surface. As shown in Figure 2.2(a), where only one of numerous
DGWs is pictured, the bottom of the DGW can be ion-implanted with the standard
Vitesse source/drain implant and contacted with a standard ohmic contact. One or
several chips are then loaded into the MBE system and the desired heterostructure is
grown, as depicted in Figure 2.2(b). A GaAs/AlGaAs LED heterostructure is shown
as a representative example. As already stated, single-crystal material grows in the
DGWs and polycrystalline material deposits in the inter-DGW regions. The chips
are then removed from the MBE system, stripped of polycrystalline deposits and the
epi-islands are processed into functional optical devices. The optical and electrical
devices are typically interconnected with the same metal as the p-type contact to the
optical device, an LED in this example. See Figure 2.2(c). Figure 2.3(a-c) is a three-
dimensional view of the same growth and processing sequence shown in Figure 2.2
(a-c). Upon completion the chips are tested and then distributed to various OEIC
users for system performance characterization. Figure 2.2 demonstrates the ease with
which multiple designs can be processed simultaneously, though all steps other than
electronic circuit fabrication can be done at a single site by a single designer.

2.2 Optoelectronic Circuit Design

The design of optoelectronic circuits to be fabricated with the E-o-E optoelectronic
integration technique can be viewed as two joint designs. One design is the electronic
circuit to perform the desired digital logic or analog function. This design follows
standard GaAs enhancement- and depletion-mode MESFET circuit design in one of
many possible logic families, direct-coupled FET logic (DCFL) for example. The
other design is the geometric layout of the DGWs. These are often placed near drive and receive circuitry, similar to electrical bond pad positioning. As previously discussed, source/drain (S/D) implants and ohmic contacts are available in the standard electronics process and are usually combined with DGWs to provide a bottom side n-type contact to the optical device. DGW orientation, with respect to the underlying GaAs crystal substrate, and DGW side wall profiles are also design parameters in addition to sizing. The first half of this section, Subsection 2.2.1, briefly presents the MESFET device model for use in the standard circuit simulation package, HSPICE [27], followed by a qualitative overview of DCFL circuit design. This review illustrates that GaAs E/D MESFET circuit design is extremely similar to silicon NMOS circuit design. The second half, Subsection 2.2.2, considers DGW and interconnection design. The combination of DCFL electronic circuits and flexible DGW layout design rules, capable of accommodating a wide range of optical devices, enables E-o-E optoelectronic circuits to achieve high performance while remaining flexible. As will be seen in Chapter 4, optoelectronic circuit applications range from high-density, low-speed arrays to medium-density, high-speed discrete transceivers. The flexibility allows the E-o-E technique to produce OEICs for this spectrum of applications.

2.2.1 GaAs MESFET Model and DCFL Design

The GaAs MESFET model presented here has been developed by Vitesse for use primarily with digital circuits [28]. It can be used for analog circuit design though the simulation accuracy for small signal device operation has not been rigorously verified. The model is parameter based and relies on a large statistical database to extract and calculate model element values. The model is accurate for MESFETs and Schottky diodes for gate lengths (L) greater than 0.8 μm and gate widths (W) greater than 2.0 μm. This discussion closely follows the model and treatment found in the Vitesse Foundry Design Manual [28] since it is the most relevant model to the E-o-E optoelectronic integration technique.
Figure 2.4 shows the MESFET equivalent circuit model used by Vitesse to describe their ion-implanted, self-aligned, refractory-gate transistor. The controlled current source determines the channel current as a function of threshold voltage ($V_{TO}$), device geometry, backgating voltage ($V_{BS}$) and the applied potentials at the source (S), drain (D), gate (G) and backgate (B) terminals. The resistances associated with the source ($R_S$), drain ($R_D$) and gate ($R_G$) represent the total series resistance between the channel and the external terminals. The gate-source capacitance ($C_{GS}$) and gate-drain capacitance ($C_{GD}$) are the voltage-dependent Schottky-barrier gate capacitances. The drain-source capacitance ($C_{DS}$) is constant and is determined primarily by the device geometry and parasitics. The backgating node factors into the calculation of the drain-source current ($I_{DS}$) but does not have an explicit physical element in this model. This model can be used to evaluate numerous terminal characteristics; however, only the current supplied by the controlled source will be discussed here. $I_{DS}$ can be analytically expressed as a function of threshold voltage, velocity
saturation effects, backgating, short channel effects and terminal biases.

The threshold voltage \( V_{TO} \) is a function of the backgating potential \( V_{BS} \), device geometry, temperature, doping concentration and the built-in voltage \( V_{BI} \) of the Schottky-barrier gate. The HSPICE MESFET model expression for threshold voltage is

\[
V_{TO} = V_{BI} - V_p
\]

(2.1)

where \( V_p \) is the pinch-off voltage and is material dependent. Since \( V_{TO} \) is a model input parameter that can be extracted from the statistical database, specific data on \( V_p \) and \( V_{BI} \) are not required for HSPICE simulations. A modified \( V_{TO} \) expression which includes the effects of bias conditions and temperature is

\[
V_T = V_{TO} + (GAMDS \times V_{DS}) + K_I(V_{BS}) - (TCV \times \Delta T)
\]

(2.2)

where \( GAMDS \) is a coefficient that accounts for \( V_{DS} \) bias dependence, \( K_I(V_{BS}) \) is a functional relationship for the backgating effect and \( TCV \) is the temperature coefficient of threshold voltage. The \( V_{DS} \) dependence is mainly due to the voltage variation of the short channel effect. \( GAMDS \) and \( K_I(V_{BS}) \) are determined by Vitesse from experimental data and an optimization routine. \( TCV \) can be measured directly, typically over the military specification temperature range of -55\(^\circ\)C to +125\(^\circ\)C, and is approximately -1 mV/\(^\circ\)C. It should also be noted that \( GAMDS \) and \( K_I(V_{BS}) \) are also dependent on device geometry, and can be included in HSPICE by providing individual parameter sets for different device sizes. All HSPICE parameters have been established for the most often used device sizes and are available to the circuit designer from MOSIS [26].

The channel current \( I_{DS} \) expression used by Vitesse is derived from recent liter-
2.2. OPTOELECTRONIC CIRCUIT DESIGN

ature [29] with some additions. The drain current is given by

\[ I_{DS} = \beta_{eff}(V_{GS} - V_{TO})VGEXP(1 + \lambda V_{DS}) \left[ 1 - (1 - ALPHA V_{DS}/3)^{SATEXP} \right] + I_{SUB} \]  

(2.3)

where the term in brackets is a polynomial form of the hyperbolic tangent function, \( ALPHA \) is the drain voltage multiplier, \( \lambda \) is the channel length modulation parameter and \( I_{SUB} \) is the subthreshold current. \( ALPHA \) determines the slope of the linear region of the \( I_{DS} - V_{DS} \) curve. While the original work [29] sets \( VGEXP = 2 \) and \( SATEXP = 3 \) these factors have been parameterized by Vitesse to provide a better fit to the measured data. The best fit gives \( 2 \leq VGEXP \leq 2.5 \) and \( 2.5 \leq SATEXP \leq 3.5 \), where any values within these ranges cause at most a 1-2% variation in the final result. Velocity saturation occurs at high gate and drain bias, where internal scattering reduces the electron mobility, and is accounted for by the expression for \( \beta_{eff} \):

\[ \beta_{eff} = \frac{\beta}{1 + VCRIT(V_{GS} - V_{TO})} \]  

(2.4)

where \( VCRIT \) is the critical field for the onset of mobility degradation. The factor \( (V_{GS} - V_{TO}) \) reduces the approximately square law \( I_{DS} - V_{GS} \) dependence at high gate biases. Together \( VGEXP \) and velocity saturation result in a slightly super-linear dependence of \( I_{DS} \) on \( V_{GS} \), \( I_{DS} \propto (V_{GS} - V_{TO})^{1.4} \), and a reduction of the transconductance. Finally, subthreshold current is modeled by Vitesse as

\[ I_{SUB} = I_0 e^{ND \times V_{DS}} e^{-NG \times V_{GS}} \]  

(2.5)

as reported in recent literature [30]. \( I_0 \) is a device geometry dependent constant and \( ND \) and \( NG \) are fitting parameters. This empirical relation has been found to agree well with measurements when \( ND \) and \( NG \) are determined using optimization techniques [28].

With the MESFET model discussed above, enhancement- and depletion-mode
MESFETs can be simulated with less than 10% error to the measured data over the entire range of applied bias. Schottky diodes can also be accurately simulated using the same model since Schottky diodes are formed by short circuiting the source and drain of a D-MESFET. Forward current flows from the gate terminal to the source-drain terminal.

There are two limitations to this model. First, gate-drain junction breakdown is not taken into account. $V_{DS}$ must be maintained at $\leq 4.5$ V at all times. The second limitation, previously mentioned, is that the simulation accuracy of small signal device operation has not been rigorously verified for this model and model values. Once again, all HSPICE [27] model and parameter files (HSPICE-decks) for circuit design in the Vitesse VLSI GaAs E/D MESFET technology are available directly from MOSIS [26].

With this basic understanding of MESFET device operation and simulation models, circuit design is straightforward. Several logic families can be implemented with the E/D MESFET technology. Source-coupled FET logic (SCFL), which can be realized using only D-MESFETs, employs series gating resulting in a very fast and efficient latch operation. SCFL also leads to a balanced circuit topology whereby the advantage of low power supply current transients is achieved. Unfortunately, SCFL requires many transistors per logic stage and also differential signal routing. While a few other logic families can address some of these SCFL shortcomings, direct-coupled FET logic (DCFL) is a popular, high-speed, high-density and nearly ideal E/D MESFET digital logic family. Therefore, DCFL is the logic style used throughout this thesis and will be the only logic family further discussed.

DCFL is the simplest logic family to implement using GaAs E/D MESFETs. Normally off enhancement-mode MESFETs ($V_T \approx +0.3$ V) are used to perform switching functions and normally on depletion-mode MESFETs ($V_T \approx -0.7$ V) are used as active loads (gate tied to source). DCFL design, like silicon NMOS design, is a ratioed logic family and performance is determined by the ratio of the transistor sizes. In
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![Circuit Diagram]

- WD/LD determined by \( I = C_L \frac{dv}{dt} \) requirement.
- WE/LE determined by restoring logic requirement.
  (Node voltage must be < VOL to achieve proper logic low.)
- Baseline speed determined by \( g_m/C_g \) of E-FET and by \( \beta \) ratio.
- \( \beta \) can be scaled to drive various capacitive loads.
- DCFL logic levels are -1.9 V low, -1.4 V high for VDD = 0.0V, GND = -2.0 V.

Figure 2.5: Summary of basic DCFL circuit characteristics. An inverter with an inverter load is shown for illustrative purposes. Figures merged from reference [28].

In other words, the relative current handling capability of the E- and D-MESFETS determines switching speeds and noise margins among other characteristics. Figure 2.5 shows the basic DCFL logic element, the inverter. The D-MESFET load element is connected between the upper voltage rail (typically 0.0 V) and the inverting output node while the E-MESFET switching element is connected between the inverting output node and the lower voltage rail (typically -2.0 V). Several switching elements (E-MESFETS) can be connected in parallel to form multiple input NOR gates, from which all other logic operations can be constructed. The DCFL logic family is characterized by low power consumption, low transistor count for a given logic function and a single power supply requirement.

A major difference between silicon NMOS and GaAs MESFET DCFL design is that the MESFET gate is a Schottky-barrier diode which draws current when it is forward biased. DCFL logic levels are -1.9 V (low) and -1.4 V (high) when the rail
voltages are -2.0 V (lower) and 0.0 V (upper). With a Schottky-barrier height of approximately 0.7 V, the DCFL high logic level (-1.4 V) approaches the Schottky-barrier height and appreciable gate current can flow. This Schottky-barrier diode is shown in Figure 2.5 as a diode load and represents the gate-source junction of the load inverter E-MESFET input device. Diode threshold is reached when the gate-source voltage of this E-MESFET reaches +0.7 V (i.e. when the gate reaches -1.3 V since the E-MESFET source is locked at -2.0 V). Though DCFL high will nominally bring this E-MESFET load gate to only -1.4 V, the actual diode current depends on the diode area and can be several hundred microamps for a wide E-MESFET. This must be explicitly accounted for in the design of DCFL gates (e.g. $\beta$ ratio is typically 10, but should be designed for specific load including diode leakage currents).

Figure 2.5 lists a few additional basic characteristics of DCFL circuitry. Among these are device scaling considerations to drive specific loads at targeted speeds and to achieve proper logic levels for cascading. This subsection is certainly not a complete description of GaAs MESFET modeling or DCFL circuit design. It is meant to be only an introductory overview to serve as necessary background for the remainder of this thesis. With the device models and circuit styles described in this subsection, it is clear that DCFL design with Vitesse VLSI GaAs E/D MESFETs is both straightforward and extremely flexible. State-of-the-art electronic circuits are routinely designed and fabricated in this manner.

The E-o-E optoelectronic integration technique accommodates arbitrarily complex electronic circuit designs. In addition to the digital or analog electronic circuits that may be on a chip for a particular application, electronic interface circuits also need to be present. These electronic interface circuits are ultimately connected to the optical devices resident in the DGWs. These electronic interface circuits which drive and receive signals onto or off of the optical devices can be thought of as the counterpart to electronic current and voltage amplifiers which drive and receive signals onto or off of electrical bond pads. In this analogy, an optical emitter and optical detector
pair form an optical input/output pad, which is the fundamental physical element for optical interconnects. Several electronic interface circuits will be presented in Chapter 4.

2.2.2 Dielectric Growth Well Design

The final aspect of optoelectronic circuit design is the layout of the DGWs and the interconnection of these DGWs to their associated interface circuitry. In actuality, the electronic circuits, DGWs and optical device fabrication masks (see Section 2.6) must be designed concurrently, but they have been artificially separated in this presentation for simplicity. While there may be several hundreds or thousands of DGWs on a chip, the design of each DGW must take into account four major considerations. For a given optical device that will ultimately reside in a particular DGW:
1. What are the physical dimensions and sidewall profile?

2. Is a particular crystallographic orientation required?

3. How should terminals be connected to electronic interface circuits and off-chip sources?

4. What on-chip optical and electrical environment is needed for optical signal access and isolation?

The remainder of this subsection will address these four design considerations in turn. Figure 2.6 shows how (a) an E-MESFET and DGW, as well as (b) a D-MESFET and DGW, are typically laid out. Figure 2.6 will be referred to repeatedly as an example of DGW design.

**1. Physical Dimensions.** An LED and an in-plane laser diode require considerably different DGW sizes. An LED is typically square with a length of a few tens of microns per side. A laser diode, on the other hand, is typically only a few microns wide but is several hundred microns long. The DGW lateral size and aspect ratio must reflect this device dependency. The term “lateral size” is used to distinguish the dimensions in the plane of the chip (e.g. X-Y) from the dimension perpendicular to the chip (e.g. Z). All DGWs have equal depths equal to the height of the dielectric stack on the chip, roughly 4.2 μm. The “lateral size” of the DGWs is a design parameter and will be referred to as the DGW size from now on.

Good quality single-crystal material has been found to grow to within approximately 5 μm of the DGW sidewall. This 5 μm perimeter contains the transition from single-crystal material to polycrystalline material against and on top of the dielectric sidewall and inter-DGW areas, respectively. DGWs should be designed at least 10 μm larger, in each dimension, than the actual optical device requires to avoid this crystal transition region.

The cross-hatched areas in Figure 2.6 represent the DGWs. Vitesse uses one etch, called the passivation etch, to remove the top overglass protective layer from the
bond pads. Until recently, Vitesse used a second etch, called the scribe line etch, to open saw lanes along which a diamond blade saw would cut the individual die apart. Upon special request, MOSIS and Vitesse will include this scribe line etch on fabrication runs. By stacking both of these standard process etches, passivation etch (also called overglass cut or mask 11) and scribe line etch (also called mask 17), the DGWs are formed as a part of the standard Vitesse fabrication run. Section 2.4 details these Vitesse etches, including typical cross-wafer etch nonuniformity and strategies to protect the GaAs crystal, as well as the remaining pregrowth DGW surface preparation etch. The layout design file containing the electronic circuit design also contains the DGW specification layers (i.e. mask layers 11 and 17). This is an essential feature and allows for convenient floor planning of the optoelectronic circuit design.

In addition to DGW size, the sidewall profile is also a design parameter. By identically sizing and aligning the passivation and street clear etches a nominally vertical sidewall is produced. If, however, the street clear etch layer is designed larger than the passivation etch layer, a sloped sidewall will result. Since the scribe lane etch occurs after the passivation etch, the sidewall profile will be slanted outward (V-groove). In the case of a circular DGW the sidewall radius would be the smallest at the GaAs crystal surface and the largest at the top overglass layer. This sort of slanted sidewall may prove beneficial in reducing the transition length between single-crystal and polycrystalline material at the DGW perimeter. Certain applications requiring angled sidewalls can also make use of this design flexibility. Angled sidewalls coated with dielectrics and metals, for example, can serve as mirrors for optical emitters (e.g. LED side emission can be deflected upward). These mirrors can also serve as deflectors to redirect optical signals for coupling into in-plane optical detectors (e.g. TM active inter-subband detectors). The angle of the two-step staircase sidewall is determined by the two etch depths and relative positioning. Section 2.4 discusses the Vitesse etch depths and Figure 2.10 is a schematic of a vertical sidewall.
Figure 2.7: Schematic illustration of the E-o-E OEIC fabrication flow (read clockwise starting from upper left). Particular emphasis is placed on wafer orientation.
2. Crystal Orientation. Certain optical devices require alignment with particular crystallographic directions. End-fire lasers with cleaved mirror facets, for example, should be aligned along cleavage planes. Another example is waveguide modulators where electrooptic effects are preferential in certain directions. Finally, all optical devices that involve wet-crystallographic etches are particularly dependent on orientation. For these reasons it is essential to orient the DGWs with respect to the underlying crystal in a manner consistent with optical device fabrication and operation.

Figure 2.7 is a schematic illustration of OEIC fabrication flow using the E-o-E technique. Figure 2.7 is intentionally quite similar to Figure 2.1, where the emphasis on MBE growth has been replaced by an emphasis on design orientation with respect to the GaAs substrate. To understand how DGWs should be oriented in the design, the various orientations and rotations throughout the electronic circuit fabrication flow must be reviewed. As seen in the upper-left panel of Figure 2.7, all transistors and DGWs are placed on a chip which is schematically represented as a square with a dagger drawn on the diagonal. All transistors (too small to be shown in the figure) have gates that are parallel to the sides of the chip (drawn square). If the chip is 5 mm on a side, for example, then the long axis of the dagger is roughly 7 mm long, which is a typical length for waveguide modulators. This dagger will be considered the DGW for a waveguide modulator, in this example, though most DGWs are of the order of tens to hundreds of microns on a side, not millimeters. This schematic also represents the orientation of the design on the computer aided design (CAD) layout system. When the chip design is completed, it is electronically transferred to MOSIS where it is placed in a reticle alongside several other designs from other universities. MOSIS can either rotate this design by 90° multiples or introduce no rotation at all. In the upper-right panel of Figure 2.7 no rotation is introduced. A special request should accompany all design submission to MOSIS specifying the desired rotation (typically no rotation). MOSIS sends the reticle design to Vitesse's
mask house where the reticle is stepped 21 times across a four-inch-diameter area as shown in the middle-right panel of Figure 2.7. This introduces no rotation. As an aside, it is conceptually simpler to think of a physical mask being produced which contains the tiled reticles as opposed to considering the possibility of Vitesse stepping a single reticle mask. Both are identical for the purposes of rotation tracking. The completed mask set (one mask for each physical layer of the design) is then sent to Vitesse. Vitesse rotates the masks 45° clockwise (looking through the mask at the substrate wafer). Recall that transistor gates were layed out parallel to the four edges of the square chip design. If Vitesse did not introduce a rotation, the transistor channels, which are perpendicular to the gates, would end up along (011) directions. This would be unfortunate because the 01\overline{1}-0\overline{1}1 direction and 01\overline{1}-0\overline{1}1 direction are not equivalent and do not have the same mobilities. This would result in some MESFETs having higher transconductances, for example, than the rest of the MESFETs. To achieve maximum uniformity, Vitesse rotates the masks, and therefore the MESFET channels, by 45° so that all MESFET channels are aligned with (001) directions. Of importance to DGW design is that the dagger ends up along the 01\overline{1}-0\overline{1}1 direction as shown in the sequence of diagrams in the lower-left panel of Figure 2.7.

With the orientations and rotations described in Figure 2.7, it is possible to orient DGWs in the design such that the optical devices are correctly oriented with respect to the underlying substrate. Returning to Figure 2.6, it is now clear that the DGW edges are in (001) directions since the edges are parallel to the MESFET gate directions which are known to end up in (001) directions.

3. Interconnection. With the DGWs sized and oriented appropriately for their respective optical devices, electrical interconnection with interface circuitry and/or with off-chip sources must be considered. Figure 2.6 illustrates both of these possibilities. A convenient scheme to connect an interface circuit with one terminal of the optical device is through an ohmic contact to a source/drain (S/D) n⁺ implanted region at the bottom of the DGW. As shown in Figure 2.6, a S/D implant region
(typically 200 $\Omega/\square$) can be produced under the DGW. In layout this is accomplished by placing an "active layer" rectangle, without gate metal as would be the case for a MESFET, in the region to be S/D implanted. Typically the S/D implant is made a few microns larger than the DGW to allow for slight misalignment, similar to via-metal design rules, as shown in Figure 2.6. The S/D region can also be made to extend into the DGW perimeter by only a few microns and rely on a heavily doped epitaxial layer to distribute current throughout the rest of the DGW area. This has the possible advantage of growing on nonimplanted material which could result in better material quality. In either configuration, at least one edge of the S/D implant should be extended enough to be contacted by ohmic contact metal (typically 0.3 $\Omega$-mm). This is shown on the left-hand side of the DGWs in Figure 2.6. Via 1 and metal 1 can be aligned to this ohmic metal to route metal 1 to an interface circuit, in this case a simple (a) E-MESFET or (b) D-MESFET in Figure 2.6. Extending the S/D implant on all four sides and making an ohmic contact ring around the DGW has the advantage of more uniform current flow to the interior of the DGW, but it has the disadvantage of increased capacitance.

If the bottom side of the optical device is n-type, but this terminal needs to be routed off-chip instead of to on-chip interface circuit, the S/D implant and ohmic contact can still be used. Instead of connecting the ohmic metal contact to metal 1 and then routing over to a MESFET, as shown in Figure 2.6, the metal 1 can be contacted by metal 2 and so forth until metal 4 is reached, which is the metal bond pads are made from. This provides a direct electric contact from a bond pad to the bottom n-type contact of the optical device in the DGW. If it is the top side of the optical device, either n- or p-type, to which a bond pad needs to be connected, then a bond pad should be designed adjacent to the DGW, as shown to the right of the DGWs in Figure 2.6. This bond pad is made from metal 4 and is electrically unconnected at the time of design. A metal interconnect line (conceptually metal 5) will eventually be run from the top side of the optical device to this pad as
part of the optical device fabrication sequence. This will be detailed in Section 2.6. There still remain two contact possibilities. First, if instead of having the top side of the optical device connected to an unconnected bond pad, the bond pad itself can be connected back down to electronic circuitry or to other bond pads or optical devices. This configuration allows the top side of optical devices to be connected to interface circuitry. The second possibility addresses bottom-side p-type contacts. Clearly these devices should not be grown on S/D implants because the n-type S/D implant would be in direct contact with the p-type epitaxy. A nonintentionally doped (n.i.d.) epitaxy layer or a low-temperature GaAs (L.T.G.) layer can be grown between the S/D implant and the p-type layers to isolate them, but it is simpler to design those DGWs with no S/D implants. Regardless, bottom-side p-type contacts require contact metallization from the top. In other words, either etching down to the p-type layers or implanting (e.g. Be) to contact the bottom-side p-type layers is required. Both of these methods are a part of the epitaxial "island" processing and mask design process, covered in Section 2.6.

4. Environment for Access and Isolation. The last consideration for DGW design is placement. Optoelectronic circuits ultimately are used in optical or optoelectronic systems. Two of the many possible systems are in-plane optical fiber coupled and large two-dimensional surface-normal array configurations. In-plane fiber coupled systems require edge-emitting lasers and edge accessible waveguides and modulators. The DGWs for these systems must either be at the edge of the chip or positioned such that the chip can be sawed or cleaved to create edge access. The spacing between the DGWs must also be designed. Optical fiber ribbons, for example, typically have a center to center pitch of 250 \( \mu \text{m} \) which can easily be matched by placing the DGWs on 250 \( \mu \text{m} \) centers. Such precise alignment (lithography-limited submicron type tolerances) is exceedingly difficult with alternate integration techniques where individual optical devices are placed.
2.2. *OPTOELECTRONIC CIRCUIT DESIGN*

The second example optical system is large two-dimensional surface-normal arrays. These systems must have their vertical emitter, detector or modulator DGWs placed on a grid matched to the off-chip optics. Surface-normal configurations typically rely on free-space optical beams (e.g. free-space optical interconnects). Such beams are often created with diffractive optical elements (DOEs), holographs or other optoelectronic arrays which have fixed spacings. Free-space beams also suffer from diffraction. These effects must be taken into account both while designing the overall optical system as well as, though implicitly already included, while designing the DGWs in the optoelectronic circuits.

In both of the example systems considered here, unwanted optical and electrical cross talk and feedback are concerns. Optical cross talk can arise from scattering, parasitic launching of optical signals into the interlevel dielectric layers (both surface normal as well as from the DGW sidewalls), beam divergence and optically induced backgating. Optical signals incident on the GaAs substrate create photogenerated electron-hole pairs which can lead to local potential fluctuations. Purely electrical cross talk can be caused by electrical line coupling as well as backgating effects. As described in Section 2.3, there is a thin p-type conductive layer just beneath all of the Vitesse MESFET electronics. This layer does not significantly contribute to backgating when a fairly high density of S/D contacts exist because the thin p-type layer is depleted. For lower density designs, however, backgating can be an issue and several measures can be taken to reduce this effect. These approaches will be discussed in Chapter 5. Optical and electric cross talk can be minimized by careful DGW and circuit design and layout. Metal 3 or metal 4 shields can be placed above electronic circuits and unused crystal to prevent stray optical signals from reaching the substrate. Metal rings, constructed from slightly offset vias, can be used to surround optical emitter and detector DGWs to reduce the effects of stray optical signals. Unwanted optical feedback is also suppressed with these shield ideas.
2.3 Electronic Circuit Fabrication

The Vitesse enhancement- and depletion-mode MESFET process is designed to produce high-performance, low power dissipation GaAs VLSI digital circuits. These characteristics are achieved by using self-aligned MESFETs and multiple levels of interconnect metallization. Refractory-metal gates and ohmic contacts are two key process innovations that allow for high-temperature post-processing. The gate metal is tungsten based while the source/drain metal is nickel based. Aluminum-based interconnects allow for high electronic integration densities and a high-yield process. Currently, three active devices are available: enhancement-mode MESFETs, depletion-mode MESFETs, and Schottky-barrier diodes. The transistors are used both as switches and as active loads and have a minimum gate-length of 0.8 \( \mu \text{m} \) in the Vitesse high-speed GaAs III (HGaaS3) process. The diodes are primarily used as level shifters. The effects of series resistance in the channel are minimized by the self-aligned process used to define the channel and contact regions. Therefore, the transistors have high transconductances and large current handling capabilities.

The process flow outlined here follows that given in the Vitesse Foundry Design Manual Version 6.0 [28] and from private communication [31]. Proprietary process information, understandably, is not disclosed. The Vitesse fabrication sequence consists of 38 major steps, and requires 13 mask levels. The substrate is a 4-inch-diameter, semi-insulating GaAs crystal which has been implanted multiple times. This proprietary implantation sequence improves threshold voltage uniformity across the wafer and leaves the substrate slightly p-type. Twenty-one reticle sites are obtained per wafer through the MOSIS service. Alignment marks and process control monitors (PCMs), which are standard electrical test structures, are outside of this reticle area [32]. The thermal-cycle, time-temperature stability study described in Section 3.1 includes these PCMs. Figure 2.8 shows the major fabrication steps and Table 2.1 details the dielectric and metal layer deposition characteristics.

Changes in device performance resulting from thermal cycles are of primary con-
Figure 2.8: Vitesse Semiconductor Corporation self-aligned ion-implanted refractory-metal VLSI GaAs E/D MESFET fabrication sequence. Table 2.1 details the dielectric and metal layer deposition characteristics. The final cross section (h) is not shown to scale and does not indicate the true top surface morphology (see Section 5.1) [28, 31].
Figure 2.9: Vitesse and Motorola VLSI GaAs E-MESFET thermal stability. (a) transconductance, $g_m$, and (b) half-channel resistance, $R_S$, vs. three-hour thermal cycle temperatures indicates that no significant changes occur below 500°C [33].
Table 2.1: Vitesse HGaAs3 dielectric (top) and metal (bottom) layer deposition characteristics (PECVD: plasma-enhanced chemical vapor deposition, RIS: reactive ion sputtering and SOG: spin on glass) [28, 31].

cern. In the E-o-E integration technique, the electronic circuits must be able to withstand the optical device epitaxial growth time-temperature sequence. In molecular beam epitaxy (MBE), which is the proposed growth system since it offers the best control of atomic layers which is critical for low-power quantum well heterostructures, a typical growth rate is roughly 1 μm per hour. Three- to five-hour growths are typical. A detailed experimental analysis of the time-temperature stability of Vitesse HGaAs3 circuits will be presented in Section 3.1, but a quick summary of the results is warranted at this time. Figure 2.9 shows two relevant transistor figures of merit, the transconductance ($g_m$) and the half channel resistance ($R_S$) for both a Vitesse 50 μm × 1.0 μm EFET and a Motorola 50 μm × 0.8 μm EFET. These parameters are plotted against the temperature at which PCM circuits were stored for three hours. Three hours is slightly less than the time it takes to align the heterostructure with the top of the dielectric side wall and five-hour thermal cycles were used for the majority of the thermal stability experiments. This storage (i.e. circuits not electrically
driven) cycle mimics an epitaxial growth sequence. A breakpoint around 500°C is clearly seen in both the $g_m$ and $R_S$ plots. This indicates that storage at temperatures above 500°C for three hours degrades performance. This time-temperature region should be avoided and E-o-E growth sequences need to be conducted at temperatures less than 500°C. As will be discussed in Section 3.1, for five-hour thermal cycles at temperatures above 500°C, a reaction at the ohmic contact sites is believed to be responsible for an increase in $R_S$. An increased $R_S$ decreases the gate-channel voltage thereby decreasing $g_m$ and related parameters such as drain-source saturation current. Finally, it turns out that the maximum five-hour thermal cycle temperature is 470°C and is determined by an interconnect metallization reaction. This is a reasonable time-temperature constraint as will be discussed in Section 2.5.

2.4 Dielectric Growth Well Preparation

After the chips are returned from the foundry (e.g. Vitesse), a pregrowth etch and clean must be performed. There is typically a fluorocarbon ($C_xF_y$) residue and a thin dielectric layer remaining at the bottom of the DGWs. SIMs analysis has revealed that the fluorocarbon layer (Teflon-like film) is extremely thin, on the order of 500 Å[34], and is a residue of the CHF$_3$/CF$_4$/O$_2$ RIE used by Vitesse to etch through the dielectric stack [31]. Most of the dielectric stack is removed in the DGW regions by stacking the passivation and scribe lane etches, but a dielectric layer ($\sim$ 1 μm) is left to protect the GaAs surface. This layer protects the crystal surface is two ways.

First, the RIE energy used by Vitesse is typically quite high and the etch uniformity is typically poor (i.e. not tightly controlled). In the case of the passivation etch, a high RIE energy is needed to quickly cut through the top overglass and expose the aluminum bond pads. A generous overetch is used to reliably open all bond pads even if the top overglass thickness and density varies significantly across a wafer. RIE etching nonuniformity is also accounted for in this manner. In the case of the optional
Figure 2.10: Artist’s perspective of three stages of dielectric growth well (DGW) pregrowth clean: (a) chips as received from Vitesse are O$_2$ reactive-ion etched (RIE) to remove residual fluorocarbons (Teflon-like film), (b) chips are patterned with photoresist (3 μm overhang to allow for ~100% overetch) to allow buffered-oxide etch (BOE) to react with the residual dielectric while protecting the sidewalls and (c) photoresist is removed revealing near-vertical dielectric sidewalls and a growth-ready GaAs surface.
scribe lane etch, rapidly etching all of the way to the GaAs substrate and possibly
damaging the surface is acceptable to Vitesse since these areas will be sawed. Once
again, an overetch is included to assure that all scribe lanes are opened. This etch was
a part of the standard Vitesse process, but it is now optional because the passivation
etch can be used to cut scribe lanes deep enough to saw die with standard diamond
blades. Therefore, the scribe lane etch is available only by special request [26] and
can be tailored. Depending on the thickness and uniformity of the dielectric left in
the DGWs after passivation etch, the scribe line etch may or may not be performed
to open the DGWs closer to the GaAs surface. It is critical that the Vitesse etches do
not reach the GaAs surface, taking etch nonuniformity into account, since the surface
will be damaged. MIT-OEIC-3/NCIPT-OEIC-1 optoelectronic circuit chips, fabric-
cated at Vitesse from November 1994 - February 1995 [58], had between ~ 0 μm and
1.5 μm of dielectric left in the DGWs after just the passivation etch (measurements
were cross-wafer). This thickness was measured at Vitesse [53] and due to the ex-
tremely thin dielectric in areas of the wafers, due to passivation etch nonuniformity,
the scribe lane etch was not performed on the majority of the wafers.

The second way that the thin dielectric layer protects the GaAs surface is that
the surface is environmentally sealed during the pregrowth storage period, which can
range from weeks to years.

Regardless of the combination of Vitesse etches used to create the DGWs, the
residual Teflon-like film and dielectric layers must be removed in preparation for
growth. Figure 2.10 (a) is a schematic illustration of the chips as received from Vitesse.
The original E-o-E demonstration chips did not have a carefully controlled dielectric
layer left in the DGWs and the Vitesse etches did reach the GaAs surface. The original
cleaning method (not shown in Figure 2.10) was to CF₄/O₂ RIE etch the entire
unpatterned chip to remove the residual Teflon-like film. Typical RIE parameters
are 45 sccm CF₄, 10 sccm O₂, 45 mTorr, 200 W, 200 V for 10 minutes at 25°C. The
chips were then etched in an ultrasonic bath of BOE for 5 minutes to thoroughly
Figure 2.11: 1000× optical micrographs (Nomarski) of crystal surfaces: (a) growth-ready bulk n⁺ GaAs sample, (b) growth-ready ion-implanted DGW (prepared using original cleaning technique), (c) after 4.2-μm-thick (Al,Ga)As LED growth on (a), and (d) after same growth as (c) except on DGW described in (b). There is no surface morphology visible in (a) or (c). There is morphology visible in (b) due to the DGW etching and cleaning technique. The morphology in (b) is accentuated after growth (d) though LEDs are functional. DGW pictured is on an MIT-OEIC-1 chip (see Section 4.6).
clean the surface of any oxides. The resulting growth-ready surface was observed to have a textured surface morphology (1000× optical microscopy with Nomarski) resembling the distribution of Teflon-like particles originally present. Presumably these particles partially shielded, and thereby patterned, the GaAs surface during RIE etches at Vitesse and/or MIT. Figure 2.11 shows 1000 × optical micrographs (Nomarski) of crystal surfaces: (a) growth-ready bulk n+ GaAs sample, (b) growth-ready ion-implanted DGW (prepared using original cleaning technique), (c) after 4.2-μm-thick (Al,Ga)As LED growth on (a), and (d) after same growth as (c) except on DGW described in (b). There is no surface morphology visible in (a) or (c). There is morphology visible in (b) due to the DGW etching and cleaning technique. The morphology in (b) is accentuated after growth (d). The DGW pictured is on an MIT-OEIC-1 chip (see Section 4.6). This original method was, however, successfully used for all of the original demonstration chips (chips found in Sections 4.1 - 4.6), though an improved method was sought.

Figure 2.10 (a) - (c) is a description of the improved DGW pregrowth clean sequence developed with J. Ahadian (Fonstad’s and Kolodziejski’s groups at MIT). As previously discussed, and as shown in Figure 2.10 (a), a Teflon-like film and a thin dielectric layer are left in the DGWs. First, O₂ RIE, which does not etch dielectric layers, is used to completely remove the Teflon-like film residue from the chip which prevents subsequent etching steps from experiencing shadowing or self-masking effects. A CF₄/O₂ RIE, which removes the existing Teflon-like deposits while etching the remaining dielectric layer, would generate additional Teflon-like residues. CF₄/O₂ RIE is, therefore, undesirable as the first RIE step. Typical O₂ RIE parameters are 75 sccm O₂, 200 mTorr, 300 W, 250 V, for ~ 90 minutes at 50°C. The second step, (b), is to pattern the chip with photoresist, leaving openings only at the bottom of the DGWs. A dielectric deposition step can precede the patterning of photoresist for added bond pad protection during cleaning and growth steps. This dielectric layer can be transparently inserted into the E-o-E process sequence because the bond pads
are often covered with electrically insulating, optical device dielectric and the bond pads are commonly opened with a via etch. A short CF$_4$/O$_2$, similar to that used in the original cleaning technique, can be used to reduce the dielectric thickness at the bottom of the DGWs. This RIE step may be necessary if the dielectric layer at the bottom of the DGWs is too thick to be removed with BOE (see next step). Small DGWs (e.g. 5 μm × 5 μm) can not accomodate large photoresist overhangs (e.g. 3 μm) which are necessary to protect the DGW sidewalls from BOE undercut. In these situations the CF$_4$/O$_2$ RIE is useful. It is important that the RIE does not reach the crystalline surface and that the photoresist is not significantly removed. Also, if appreciable Teflon-like residue accumulates during this step, an additional O$_2$ RIE clean is required.

The chips are then submerged in BOE which etches dielectric but does not damage the GaAs substrate. A 100% overetch is desirable to ensure that the dielectric has been removed from the bottom of all DGWs across the chip. The sidewalls are protected during this etch by photoresist. A 3 μm photoresist overhang at the edges of the bottom of the DCWs allows for the 100% overetch of the ~1.5 μm maximum dielectric thickness in the DGWs (e.g. 1.5 μm vertical etch × 200% → 3.0 μm lateral undercut). The final step is to strip the photoresist with acetone and O$_2$ RIE. It is critical that all organics are removed from the chips before they are loaded into the ultrahigh-vacuum, extremely clean MBE system. Figure 2.10 (c) illustrates the growth-ready chip. Preliminary growths using this improved cleaning technique have shown improved surface morphology, presumably because the GaAs surface was never exposed to RIE.

2.5 Lowered-Temperature Molecular Beam Epitaxy

After optoelectronic circuits have been designed and the electronic portion of the
Figure 2.12: Energy band gap versus lattice constant for common elemental and compound semiconductors. The tie lines joining the binaries represent ternary compositions. The dashed lines represent indirect bandgap materials. The horizontal and vertical dotted lines represent the InGaAlAs and InGaAsP quaternary systems, respectively. Both systems contain compounds that are lattice matched to GaAs and are compatible with the E-o-E integration technique. So too does the quaternary InGaAlP system, which is not shown explicitly, but which can be inferred from the points AlP and $\text{In}_{0.51}\text{Al}_{0.49}\text{P}$ points.
chips has been fabricated at the commercial foundry, optical devices must be grown on the chips. The E-o-E integration technique places two constraints on the epitaxial material and growth technique. First, the optical material must be lattice-matched (relaxed buffers discussed in Section 3.1.4) to the GaAs electronic circuit substrate. Second, this entire optical heterostructure must be grown within the thermal budget determined by the electronic circuits. This has been determined to be up to five hours at a maximum temperature of 470°C. These constraints can be readily met with the proper choice of material system and epitaxial growth technique. This section will begin by presenting two lattice-matched material systems which can be used with the E-o-E technique, followed by a brief overview of the epitaxial growth technique used in this work, namely molecular beam epitaxy (MBE). Procedures specific to MBE growth on electronic circuits will conclude this section.

A plot of the InGaAlAs and InGaAsP material systems energy gap vs. lattice constant is shown in Figure 2.12. Certain compositions within these material systems are both direct band gap, essential for the active regions of optical emitters, and lattice matched to GaAs. GaAs has a lattice constant of 5.654 Å. As can be seen from Figure 2.12, (Al,Ga)As is essentially lattice matched to GaAs for all compositions (i.e. Al_xGa_{1-x}As for 0 ≤ x ≤ 1). Certain compounds within the quintinary (In,Ga,Al)AsP material system are also lattice-matched to GaAs. Two compositions require only three elements, In_{0.49}Ga_{0.51}P and In_{0.51}Al_{0.49}P, which are particularly suitable for growth. Both the (Al,Ga)As and the lattice matched compounds within the (In,Ga,Al)AsP material systems are compatible with the E-o-E thermal budget constraints and can produce high-quality optical devices. There are benefits and drawbacks with both of these material systems.

(Al,Ga)As is the most mature III-V material system, which simplifies growth and process development for use in the E-o-E optoelectronic integration technique. (Al,Ga)As also spans a relatively large refractive index range, which is advantageous for achieving good optical-mode confinement and high distributed Bragg reflector
(DBR) reflectivities with thin superlattice stacks. Optical device performance is excellent, especially by including strained active layers (e.g. In\textsubscript{0.2}Ga\textsubscript{0.8}As) to enhance optical and electrical properties. (Al,Ga)As optical devices do not necessarily limit E-o-E optoelectronic circuits. On a practical note, (Al,Ga)As is also a relatively safe material system because it can be grown with solid elemental sources, as opposed to gaseous sources, which pose a significant health and environmental hazard.

Unfortunately, (Al,Ga)As is conventionally grown at temperatures in excess of 600°C. Aluminum layer quality degrades significantly below this temperature [35, 36, 37]. Numerous growth techniques have been pioneered in the past five to ten years which address this problem. A detailed discussion of the Al degradation mechanisms and designs which minimize the effects of reduced quality Al containing layers on device performance will be presented in Chapter 4.

A brief summary of laser diode threshold current densities, representative of optical emitters and epitaxial layer quality in general, is shown in Figure 2.13. Laser designs (a) - (c) are (Al,Ga)As based while (d) is (In,Ga)P based. One approach to minimizing the effects of poor AlGaAs layer quality is to pull these layers back away from the active region as far as reasonable optical mode confinement will allow. This approach was suggested by Wang et al. [38] and was extended in this work as shown in panel (a). While threshold current densities became high as the growth temperature was reduced to 530°C, threshold currents of less than 10 mA and threshold voltages of less than 1.5 V were demonstrated for integratable laser diode sizes (e.g. 4 \mu m \times 500 \mu m) [23, 24]. Though the growth temperature was higher than desired, which would begin to compromise the electronic circuit performance, these laser diodes could be driven by MESFET current amplifier stages with conventional DCFL rail voltages of 0.0 V and -2.0 V. To further decrease threshold current densities the As overpressure during MBE growth was reduced. Wang et al. [39] achieved this by repeatedly opening and closing the As shutter. Panel (b) shows that at a substrate (growth) temperature of 500°C, J\textsubscript{th} is approximately 1 kA/cm\textsuperscript{2}. While these
results are good, the temperature is still too high for the E-o-E technique. Miyazawa et al. [40, 41] carefully controlled the As beam pressure such that a near unity III/V flux ratio was produced. The source purity was also high following a lengthy high temperature bake of the MBE machine. Threshold currents of 600 A/cm² were reported at a growth temperature of 375°C. This is ideal for the E-o-E technique. Such accurate control of the As overpressure is currently being pursued in Fonstad’s group at MIT. A final approach to low-temperature lasers is migration enhanced epitaxy (MEE) by which pulses of group III followed by pulses of group V elements impinge on the substrate every monolayer. Control of these pulses is quite challenging though excellent material results [42, 43, 44].

The (In,Ga,Al)AsP material system is rapidly maturing and growth and process protocols are well understood. While optical and electrical properties of certain devices benefit from including In₀.₅₁Al₀.₄₉P layers, several high performance devices can be grown with only GaAs, In₀.₄₉Ga₀.₅₁P and often an In₀.₂Ga₀.₈As active region. State-of-the-art laser diodes and LEDs have been grown with just these three layers. The advantage of not including Al-containing layers is that a much reduced growth temperature can be maintained throughout the growth of the optical device. In₀.₄₉Ga₀.₅₁P is optimally grown at 470°C. GaAs and In₀.₂Ga₀.₈As can also be grown at 470°C without the need for unconventional growth techniques. Laser diodes with threshold current densities as low as 72 A/cm² have been grown at temperatures below 500°C [45, 46].

There are two drawbacks to the (In,Ga,Al)AsP material system. First, there is a relatively small refractive index range spanned and, second, phosphorus is most commonly used in its gas phase. A promising alternative is to use high-purity solid-phase P in a vacuum cracker source cell which effectively mimics the gas source systems.

From this discussion it is clear that E-o-E optoelectronic circuits can benefit from both (Al,Ga)As- and (In,Ga,Al)AsP-based optical devices. Both material systems should be pursued and the relative benefits and drawbacks should be further in-
<table>
<thead>
<tr>
<th>(a)</th>
<th>(b)</th>
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<tbody>
<tr>
<td>100 A Be In(0.20)GaAs</td>
<td>1000 A Be GaAs</td>
</tr>
<tr>
<td>1000 A Be GaAs</td>
<td>1.3 um Be Al(0.55)GaAs</td>
</tr>
<tr>
<td>1.4 um Be Al(0.20)GaAs</td>
<td>1200 A Al(0.30)GaAs</td>
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<tr>
<td>2000 A Al GaAs</td>
<td>120 A Al GaAs</td>
</tr>
<tr>
<td>60 A Al In(0.20)GaAs</td>
<td>1200 A Al(0.30)GaAs</td>
</tr>
<tr>
<td>2000 A Al GaAs</td>
<td>1.3 um Si Al(0.55)GaAs</td>
</tr>
<tr>
<td>1.4 um Si Al(0.20)GaAs</td>
<td>1.0 um Si GaAs</td>
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<tr>
<td>0.5 um Si GaAs</td>
<td>Si GaAs</td>
</tr>
<tr>
<td>Si GaAs</td>
<td>Reduced Aa/Ill ratio by shuttering, Wang et al.</td>
</tr>
<tr>
<td>Tsub=600C, Jth=0.74 kA/cm²</td>
<td>Tsub=500C, Jth=1.0 kA/cm²</td>
</tr>
<tr>
<td>Tsub=530C, Jth=1.80 kA/cm²</td>
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<th>(c)</th>
<th>(d)</th>
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<tr>
<td>0.5 um Be GaAs</td>
<td>— um Be GaAs</td>
</tr>
<tr>
<td>1.5 um Be Al(0.50)GaAs</td>
<td>— um Be GalnP</td>
</tr>
<tr>
<td>500 A Al(0.30)GaAs G</td>
<td>1000 A GaAs</td>
</tr>
<tr>
<td>60 A Al GaAs</td>
<td>60 A In(0.25)GaAs</td>
</tr>
<tr>
<td>500 A Al(0.30)GaAs G</td>
<td>1000 A GaAs</td>
</tr>
<tr>
<td>1.5 um Si Al(0.50)GaAs</td>
<td>— um Si GalnP</td>
</tr>
<tr>
<td>1500 A Si SL (Al,Ge)As</td>
<td>— um Si GaAs</td>
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<tr>
<td>0.5 um Si GaAs</td>
<td>Si GaAs</td>
</tr>
<tr>
<td>Si GaAs</td>
<td>Al free, gas-source GalnP cladding, Pessa et al.</td>
</tr>
<tr>
<td>Tsub=650C, Jth=400 A/cm²</td>
<td>Tsub(GalnP,InGaAs)=500C, Tsub(GaAs)=590C</td>
</tr>
<tr>
<td>Tsub=375C, Jth=600 A/cm²</td>
<td>Jth=72 A/cm²</td>
</tr>
</tbody>
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Figure 2.13: Four techniques to achieve low growth temperature lasers. All measurements are at room temperature.
vestigated. All devices presented in this thesis are (Al,Ga)As based, though the In\(_{0.49}\)Ga\(_{0.51}\)P-GaAs-In\(_{0.2}\)Ga\(_{0.8}\)As material system has been qualified and preliminary devices have been fabricated for use with the E-o-E integration technique. This work was of a collaborative nature with Joseph A. Ahadian (Fonstad and Kolodziejski groups at MIT) and the results are detailed in J. Ahadian’s masters thesis [47].

Before discussing the unique features of growing epitaxial layers on fully processed integrated circuits, it is necessary to review the growth system. There are several growth systems capable of depositing individual atomic layers of semiconductor crystal on a substrate crystal. Molecular beam epitaxy (MBE) is one such system which offers unparalleled control over growth parameters, such as compositional control and in-situ diagnostics. As the name suggests, atomic beams provide the constituent epitaxial elements. These beams are restricted to the molecular flow regime and thus require an ultrahigh-vacuum (UHV) chamber. In solid-source MBE, molecular beams are thermally evaporated from crucibles containing elemental sources that are solid or liquid at room temperature. The absolute and relative beam fluxes are controlled by varying the crucible temperatures and the flux is modulated by shutters. All (Al,Ga)As growths presented in this thesis were grown by solid-source MBE. Gas-source MBE, which uses feed gases, was used for the preliminary work on (In,Al,Ga)P heterostructures.

A schematic of the Riber 2300 MBE system used in this work is shown in Figure 2.14. UHV conditions are achieved and maintained in the growth, preparation, and loading chambers with various combinations of pumps and baking sequences. The loading chamber turbo pump achieves roughly \(10^{-9}\) Torr. The preparation chamber ion pump achieves roughly \(10^{-10}\) Torr. The growth chamber uses a cryopump, an ionization pump, a titanium sublimation pump and liquid-nitrogen-cooled shrouds to achieve a mid to high \(10^{-11}\) Torr vacuum. Such UHV conditions assure minimal epitaxial layer contamination.

The substrate manipulator, located in the center of Figure 2.14, performs five
Figure 2.14: Molecular beam epitaxy (MBE) system. Figure from reference [48] and modified.
major functions. First, the manipulator holds the molybdenum block to which the substrate crystal is indium soldered. Second, the manipulator holds a heater which controls the substrate temperature. Third, an ion gauge which monitors beam fluxes is mounted on the manipulator and, fourth, the manipulator rotates the substrate which increases lateral thickness and compositional uniformity of the growing films. Finally, the manipulator rotates from loading/unloading position, through flux measurement position, and on to growth position.

The effusion cells, also called source cells, are located in the source flange, on the far left of Figure 2.14. The elemental sources are contained in boron nitride crucibles and are heated by titanium heater filaments. Each cell has a thermocouple, PID controller, and power supply to accurately control source temperatures. Each cell also has a small circular molybdenum shutter, which either blocks or passes the beam flux. All shutters and cells are under computer controlled.

To monitor growth and vacuum conditions there are several diagnostic instruments built into the system. A reflection high-energy electron diffraction (RHEED) gun yields information on the quality and state of the substrate and epitaxial material by displaying glancing-angle electron diffraction patterns on a phosphor screen. A quadrupole mass spectrometer (QMS), also called a residual gas analyzer (RGA), yields elemental pressure information by monitoring mass-to-charge ratios. There are also numerous ion flux/pressure gauges which measure chamber pressures and beam fluxes. An infrared pyrometer (not shown) supplements the molybdenum block thermocouple temperature reading.

The final aspects of optical device MBE growth are how individual chips are mounted during growth and the specific growth sequence. After the chips are received from the foundry they can be electrically probed to verify circuit functionality. Then, in preparation for growth, the S/D n⁺ implanted GaAs at the bottom of the DGWs is cleaned as detailed in Section 2.4. The chips are then degreased and mounted with indium on a molybdenum block around the perimeter of a quarter wafer of bulk
Figure 2.15: Photograph of a molybdenum block with six optoelectronic chips surrounding a quarter wafer of bulk $n^+$ GaAs after optical device growth. Only the largest DGWs are visible on the chips, seen as dark rectangular and square areas.
2.5. LOWERED-TEMPERATURE MOLECULAR BEAM EPITAXY

n⁺ GaAs which serves as a pyrometer source, RHEED crystal and control sample. Figure 2.15 shows six optoelectronic chips arranged around the quarter wafer of GaAs.

The block is mounted in the load lock and transferred into the preparation chamber where it is outgassed at 300°C for 15 minutes (ramped up and down at 15°C/min.). After transferring the outgased block into the growth chamber the block temperature is ramped at 15°C/min. up to 600°C until the native oxide on the bulk GaAs is desorbed. Five minutes later the native oxide in the DGWs is assumed to be desorbed. This time is short enough to not significantly affect the MESFETs but it does impact the tungsten-plated aluminum interconnect metallization. This will be discussed further in Section 3.1.

As a brief aside, two low-temperature native oxide desorption techniques appear quite promising and would avoid the short, high-temperature excursion necessary for thermal oxide desorption. First, low-temperature hydrogen-plasma native oxide removal [49, 50] is possible and is being pursued in Fonstad's and Kolodziejski's groups at MIT. Preliminary growths using hydrogen-plasma appear encouraging and LEDs have been demonstrated on bulk GaAs [51]. By removing the native oxide with atomic hydrogen while the sample is held at roughly 300°C for roughly 10 minutes, the circuits would not degrade. Another method of low-temperature oxide removal is to passivate an oxide-free GaAs surface (e.g. after an HF dip) with hydrogen (e.g. residual hydrogen from the HF dip). This is an analogus technique to the native oxide removal method used for epitaxial growth on silicon substrates. After the dip the sample is hydrophobic and can be rinsed with DI H₂O. A native oxide will not form as long as hydrogen passivates the GaAs surface. The sample can be loaded into a preparation chamber where the hydrogen is driven off below 400°C, leaving an oxide-free, growth-ready surface. Preliminary tests, in Fonstad's group at MIT, using this idea appear encouraging (e.g. excellent RHEED pattern after hydrogen was driven off at 400°C) [52].

After the native oxide is removed, using any of the aforementioned techniques, n⁺
GaAs growth is initiated and the temperature is ramped down to the growth temperature (e.g. 470°C). The desired optical heterostructure is grown at this temperature with a lowered As overpressure, in the case of (Al,Ga)As. The exact growth time depends on the material growth rate and is adjusted to align the top surface of the heterostructure with the top of the DGW sidewall. A total growth thickness of 4.2 μm and a total growth time of 4.5 hours is typical. Often the first material grown on the chips is a strained-layer superlattice to trap defects. Single-crystal material grows in the windows and polycrystalline material deposits on the top overglass and bond pads. An approximately 5-μm-wide transition region, between good quality single-crystal material and polycrystalline material, occupies a ring inside the perimeter of the DGWs.

After the growth is complete, the sample temperature is ramped down at 15°C/min. and the block is removed from the chambers. The chips are dismounted and the backside indium is stripped with near boiling 1:1 HCl:DI H₂O. The optoelectronic circuit chips are then ready to be processed, yielding optical devices in the DGWs.

2.6 Epitaxial “Island” Processing and Mask Design

The major difference between processing bulk epitaxial wafer samples and E-o-E chips is that the former are typically larger than a square centimeter and the later are not. Up to this point in the E-o-E process the physical size of the electronic chips or wafers has not been of concern. Now it is. It is often convenient and cost effective to commercially fabricate chips that are as small as 2.5 mm × 2.5 mm. This is reasonable because with VLSI density circuits several fairly complex designs can be layed out in this area. This is also a reasonable size for the E-o-E technique since the DGWs can be as small as a few tens of square microns or as large as the entire chip. However, 2.5 mm × 2.5 mm chips are nearly impossible to handle when processing
Figure 2.16: Photograph of spin chuck and planar cuff used to process 4.7 mm × 4.7 mm optoelectronic chips. Top: spin chuck fully assembled (chip would reside in center above vacuum port). Bottom: spin chuck disassembled.
the epitaxial "islands" due to photoresist buildup at the edges and in the corners as well as decreased alignment accuracy with smaller alignment mark separations. For small chips "processing cuffs" can mimic larger chips by effectively extending a planar region around the chip. Such "processing cuffs" can be created by abutting other sacrificial chips or crystals of the same height around the real chip. Another approach is to machine a metal cuff, with the exact thickness of the chip, to fit around the chip and attach to the underlying spin chuck. The spin chuck with cuff used throughout this work is shown in Figure 2.16. Larger chips, at least 5 mm × 5 mm, ideally with a ≥ 1 mm or larger unpatterned border around the design to collect photoresist edge buildup, are ideal. Much larger chips or even wafers can be processed in the same manner. The upper size limit is currently set by the growth reactor, typically 2-inch-diameter samples for research MBE systems. However, 4-inch-diameter commercial MBE systems do exist and would allow the E-o-E technique to be extended to processing full 4-inch wafers.

Fortuitously, there is one significant benefit of processing small chips. This benefit is that all mask layers can be arrayed on a single 4-inch quartz plate, thus minimizing processing costs. Figure 2.17 illustrates this approach. The same CAD system that was used to design the optoelectronic chip can be used to design the optical device processing mask set. This is convenient and allows the mask set to be locked to the chip design. After the mask set is complete, the individual mask layers can be "slid" into elements of an array. The entire array must fit in the central portion of the mask to allow the mask to be moved on the aligner and still access all mask layers. Layers too close to the edge would always be exposed at an oblique angle. Another array consideration is that each layer must also take into account the edges of the chip, which likely do not contain electrical circuit but still need to be processed. Removing the polycrystalline deposits on these chip edges is an example. The entire mask set can be e-beam written on a single quartz plate for roughly $1000.

Typical layers for an LED flow are labeled in Figure 2.17. The "DGW clean" layer
Figure 2.17: Optical device processing mask scheme for use with E-o-E integration technique. (a) Optoelectronic chip design layout. (b) Optical device mask which has features only in the epi-island/DGW areas. (c) Final placement of all mask layers, side by side, on a single e-beam-written quartz plate.
can be used to develop out photoresist in the DGWs before growth. DGWs can be wet-chemical etched to finish cleaning them to the GaAs surface without damaging the Al bond pads. The “Poly Strip” mask is used to coat the epi-islands (DGWs after growth) with photoresist. The photoresist is typically extended 5 μm around the perimeter of the epi-islands. The polycrystalline material on the overglass and bond pads can be wet chemically etched (e.g. 1:1:5 H₃PO₄:H₂O₂:H₂O) until the original color of the overglass is restored, confirming that the polycrystalline material has been removed. Since the polycrystalline material is typically 5 μm thick, the 5 μm overhang of the “Poly Strip” mask around the epi-islands will be undercut since polycrystalline material etches isotropically. A nominally planar surface results after photoresist strip. The “Mesa Etch” layer allows current confining wet or dry etched mesas to be created in the epi-islands. Alignment marks are also typically written in selected epi-islands for all future alignment. Previous mask layers can be aligned to alignment marks designed into the optoelectronic chip in metal 3, for example. A dielectric layer is usually deposited over the entire chip and this needs to be removed everywhere except for over the epi-islands. Often the “Poly Strip” mask can also be used for this purpose, though a separate layer can be created if different features are needed. “Extra #1” and “Extra #2” represent slots for extra layers such as this. “Via Etch” is a layer that allows contact metal vias to be cut through the deposited insulating dielectric. As an aside, this layer can simultaneously cut vias and strip dielectric off of the inter-DGW regions if the etch time is monitored carefully. An “Ion Implant” current confinement layer is sometimes used. The final layer is “Metal Liftoff” and makes top-side ohmic contacts (e.g. p-type contacts) to the optical devices as well as electrical interconnects to nearby bond pads. The interconnection metal is termed metal 5 since it is the next metal layer after Vitesse metal 4. This completes the epi-island processing flow and the optoelectronic circuits are now ready for characterization.
At last the optoelectronic circuits can be characterized. Figure 2.18 is an optical microphotograph of an epi-island with twenty fully fabricated LEDs. The LEDs have a common n-type S/D contact which is connected to the interface circuit (above the epi-island) with an ohmic/metal 1 contact. The top-side p-type contact for 19 out of 20 of the LEDs should be directly microprobed and the optical signal monitored. The final LED has its p-type contact connected over to a bond pad (below the epi-island). If the chip is mounted in a package (e.g. DIP or PGA) this pad, as well as the pads associated with the electronic circuit, can be bonded to the package pins. A packaged chip awaiting bond wires is shown in Figure 2.19. At this point the optoelectronic circuits are ready to be introduced into the optical system for characterization. Optical systems can be as simple as an optical power meter to measure the LED optical power vs. drive current characteristics. It is important to recall that LEDs are just one of a variety of optical devices that can be integrated. Chapter 3 describes in detail the
full range of optical devices that either have been or are capable of being integrated. Chapter 4 presents several demonstration optoelectronic circuits fabricated with the E-o-E technique. The full range of optoelectronic circuits and subsystems possible with the E-o-E optoelectronic integration technique will then be apparent.
Chapter 3

Devices for E-o-E OEICs

The previous chapter detailed the E-o-E technique which can be used to monolithically integrate a wide variety of optical devices with electrical circuitry. This chapter presents several electrical and optical devices which are compatible with the E-o-E integration technique and, therefore, can be included in E-o-E optoelectronic circuits. Most of these devices have been designed and experimentally demonstrated as part of this work. Several other devices are included in this discussion because they are well positioned for use in E-o-E OEICs. This library of electrical and optical devices is organized as follows: Section 3.1 discusses the thermal stability of the Vitesse E/D MESFET process electrical devices, Section 3.2 covers optical detectors, Section 3.3 presents optical emitters and Section 3.4 overviews optical modulators. Numerous electrical and optical devices, not covered in this chapter, are undoubtedly also compatible with the E-o-E integration technique.

3.1 Electrical Devices (Thermal Characterization)

The elevated temperature stability of Vitesse Semiconductor's HGaAs2 and HGaAs3 process was characterized for application in the Epitaxy-on-Electronics (E-o-E) optoelectronic integration technique. HGaAs3 is the current Vitesse process and re-
placed the HGaAs2 process approximately two years ago (1993). For this reason, only HGaAs3 thermal characterization results will be presented here. HGaAs2 results were previously reported [24, 54] and are quite similar to HGaAs3 thermal stability results. The HGaAs3 thermal stability study was conducted in collaboration with Eric K. Braun [55] at MIT and is detailed in E. Braun’s masters thesis [56] as well as in a submitted publication [57]. Before presenting the thermal stability findings, for both passive and active devices, the measurement and thermal cycling procedures will be briefly described. All measurement procedures and defined parameters are consistent with internal Vitesse protocols to facilitate comparisons [32].

Electrical test structures located on Vitesse HGaAs3 process control monitor (PCM) test bars were measured before and after elevated temperature thermal cycles. The sheet resistances of gate metal, ohmic metal and interconnect metal, levels 1 through 3, were determined by the measurement of metal snake resistors. Metal-to-metal and metal-to-implant resistances were determined from contact string resistor measurements. Large and small transmission line model (TLM) structure resistance measurements allowed the extraction of the ohmic contact resistance ($R_C$) and implant sheet resistance ($R_{SH}$). I-V characteristics of enhancement and depletion metal semiconductor field effect transistors (MESFETs) of varying length and width were measured and the threshold voltage ($V_T$), transconductance ($g_m$), saturation current ($I_{DS sat}$), and source resistance ($R_S$) was extracted for each of 9 different devices. In addition, Schottky-barrier heights ($\phi_b$) and ideality (n) were extracted for 3 different DFETs. Lastly, the oscillation period of a 23-stage direct coupled FET logic (DCFL) ring oscillator with beta ratio ($\beta$) of 10 was measured.

The MESFET threshold voltage is a measure of the gate bias, $V_{GS}$, required to create a minimally conducting channel. A $V_{DS} = 0.15$ V bias was applied, $V_{GS}$ was ramped up and the resulting $I_{DS}$ was measured. $I_{DS}$ vs $V_{GS}$ was then plotted and the linear region, with maximum slope, was extrapolated to the $V_{GS}$ axis. This intercept is termed $V_{GS intercept}$. A defined threshold voltage was calculated using $V_T$
3.1. ELECTRICAL DEVICES (THERMAL CHARACTERIZATION)

\[ V_{GS_{\text{intercept}}} - \frac{V_{DS}}{2}. \]

The MESFET drain-source saturation current is a measure of the maximum current that can flow through the channel. \( V_{GS} = 0.5 \) V and \( V_{DS} = 1.0 \) V were applied and the resulting \( I_{DS}^{\text{sat}} \) was measured.

The MESFET transconductance is a measure of how effectively \( I_{DS} \) is controlled by \( V_{GS} \). \( g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \) for \( V_{DS} \) held constant assuming no voltage drop across the gate-drain and gate-source regions. A \( V_{DS} = 0.15 \) V was applied to the MESFET and \( V_{GS} \) was ramped up. The derivative of \( I_{DS} \) with respect to \( V_{GS} \) was plotted and the maximum value is referred to as simply \( g_m \) from now on.

The MESFET series resistance is a measure of the resistance in the channel of the FET. \( R_S \) was measured by forward biasing the gate-source junction and then measuring the drain-source voltage, \( V_{DS} \). To stabilize the measurements, a small \( I_{DS} \) (1 \( \mu \)A) was driven through the MESFET channel from drain to source. This current does not add a significant voltage to \( V_{DS} \) and thus the calculated \( R_S \) was not significantly affected. \( V_{GS} \) was ramped up and the measured \( V_{DS} \) values were plotted against the measured \( I_{GS} \). \( R_S \) is equal to the slope of the resulting line.

The MESFET gate-(source/drain) ideality and barrier heights are measures of the gate-(source/drain) diode quality. The source and drain contacts were both grounded and the gate bias, or equivalently diode bias (\( V_D \)), was ramped up. A plot of \( \log(I_D) \) vs. \( V_D \) was then created and the maximum slope and the extrapolated \( \log(I_D) \) intercept were determined. From these two values the diode ideality and barrier height were calculated as follows:

Thermionic emission dominated Schottky-barrier current (\( I_D \)) is given by

\[ I_D = A^* A T^2 e^{-\frac{\phi_b}{kT}} e^{\frac{V_D}{n kT}} \]  \hspace{1cm} (3.1)

where \( I_D \) is the diode current, \( A^* \) is Richardson’s constant, \( A \) is the diode area, \( \phi_b \) is the barrier height, \( V_D \) is the applied diode voltage, \( k \) is Boltzman’s constant, \( T \) is the temperature in kelvins, \( q \) is the charge on an electron and \( n \) is the ideality factor.
From Equation 3.1 it can be shown that

\[
\log(I_D) = \log(A^*AT^2) + 0.434\left(\frac{-\phi_b}{kT}\right) + 0.434\left(\frac{qV_D}{nkT}\right) \quad (3.2)
\]

where the prefactor of 0.434 accounts for the base 10 logarithm. The sum of the first two terms in Equation 3.2 is equal to the \(\log(I_D)\) intercept on the \(\log(I_D)\) vs \(V_D\) plot. The third term in Equation 3.2 is equal to \(V_D\) times the slope of the \(\log(I_D)\) vs \(V_D\) plot. For the diodes measured, \(A = 1.5 \times 10^{-7}\) cm\(^2\). The effective Richardson constant \(A^*\) was extracted from a \(\log(I_{DS})\) vs \(1/T^2\) plot and was found to be \(52\) A/cm\(^2\)K\(^2\) [32]. \(T = 300\) K and \(k = 1.38 \times 10^{-23}\) J/K are also known. From these values it can be shown that

\[
\phi_b = \frac{-(\log(\text{intercept}) + 0.15366)}{16.79} \quad (3.3)
\]

\[
n = \frac{16.76}{\text{slope}} \quad (3.4)
\]

The MESFET contact resistance is a measure of the ohmic contact metal to source/drain N\(^+\)-implant junction resistance. The N\(^+\)-region sheet resistance is a measure of the dopant concentration and the electrical conductance. Three rectangular metal pads with two different spacings is collectively termed a TLM structure. A current source was used to force 15 mA through two electrodes and the resulting voltage across two monitor electrodes was measured. This was performed for both TLM contact spacings, each yielding a resistance. These two resistances were then plotted as a function of the electrode spacings. The slope of the resulting line multiplied by the ohmic contact width is the sheet resistance of the N\(^+\) implant regions. The R-axis intercept is \(2R_C\), where \(R_C\) is the contact resistance.

The thermal cycles were conducted in a quartz tube, sealed with end-caps, heated by a cylindrical furnace. After a chip containing a PCM was loaded into the quartz tube, the tube was evacuated and backfilled with nitrogen gas. Nitrogen was flowed at a rate of approximately 2 sccm throughout the thermal cycle to minimize oxidation of
the aluminum bond pads. This system was designed to mimic the MBE environment in which the electronic circuits will reside during E-o-E epitaxial growth. Several chips, which served as controls, were thermal cycled in an MBE reactor and compared with furnace cycled chips. The extracted parameters agreed quite well and were within the difference accounted for by the temperature uncertainties (furnace temperature was monitored with a thermocouple and the MBE sample temperature was monitored by both a thermocouple and an infrared pyrometer focused on a GaAs crystal next to the chips).

The chips were ramped in the furnace from room temperature to the maximum thermal cycle temperature in 0.5 hours, maintained at the maximum temperature for 5.0 hours, and then ramped back to room temperature in 1.0 hour. These times correspond approximately to a 4.2 μm MBE heterostructure growth sequence. The maximum temperature was varied between 400°C and 600°C which are typical lowered-temperature (Al,Ga)As and (In,Ga)P MBE growth temperatures.

The following subsections present thermal stability results for all process and device structures relevant to the E-o-E integration technique: metal interconnects (Subsection 3.1.1), ohmic contacts and resistors (Subsection 3.1.2) and enhancement- and depletion-mode MESFETs including Schottky diodes (Subsection 3.1.3). The final subsection (Subsection 3.1.4) briefly describes one possible class of electronic devices which can be monolithically integrated, resonant tunneling diodes (RTDs). While the E-o-E integration technique may be primarily used to intermix optical devices with electronic circuits, it may also be used to integrate electronic devices such as heterostructure field effect transistors (HFETs) or RTDs with GaAs VLSI MESFET circuits.

3.1.1 Metal Interconnects

Figure 3.1 shows the gate metal, ohmic metal and interconnect metal 1 through 3 sheet resistances as a function of 5-hour thermal cycle temperature. The gate metal
Figure 3.1: Vitesse HGAs3 metal layer sheet resistance before (far left) and after 5-hour thermal cycles [57].

consists of 3500 ÅWNₓ deposited over the channel implant. The ohmic metal consists of 700 ÅNiGe deposited over the source/drain (S/D) implant followed by a 1000 ÅWNₓ barrier. The metal 1 through metal 3 layers are a WNₓ/AlCuₓ/WNₓ sandwich with thickness ranges of (1000 Å- 1500 Å)/(8000 Å- 17000 Å)/(1000 Å), respectively. The WNₓ contains 10-20 atomic percent nitrogen and the AlCuₓ contains about 1% copper.

Figure 3.1 provides a strong indication that there are no large scale metallurgical reactions between WNₓ, NiGe, GaAs and the SiO₂ passivation for up to 5 hours at 600°C. However, the aluminum-containing metal 1 through 3 layers showed a striking sheet resistance increase after 5 hours in the temperature range of 475°C to 550°C. This resistance increase is believed to be the result of a metallurgical reaction between the AlCuₓ core and the WNₓ claddings (AlCuₓ + WNₓ → Al-Cu-W-N). Reaction between Al and WNₓ has been previously reported to occur at temperatures as low as 500°C.
3.1. ELECTRICAL DEVICES (THERMAL CHARACTERIZATION)

Figure 3.2: Metal 1 sheet resistance thermal cycle response Arrhenius-based model (activation energy \( \approx 3.5 \text{ eV} \)) \[57\].

\[59\] with reaction products including Al\(_{12}\)W and AlN.

The metal 1 sheet resistance increases linearly in time with thermal activation energy \(3.5 \text{ eV}\) before saturating at approximately 15 times the sheet resistance before thermal cycle. Based on an Arrhenius model, a curve set was fitted to the measurements to predict the metal 1 sheet resistance for arbitrary times in the temperature range 400°C to 600°C. Figure 3.2 shows this model with excellent agreement to experimental measurements from 5 minutes at 600°C to 1 week at 475°C.

The thermal response of WN\(_x\)/AlCu\(_x\) layers with increased nitrogen content, WN\(_x\), was investigated by adjusting the tungsten sputtering rate with constant nitrogen flow rate. This process variation was performed at Vitesse \[31\] on standard aluminum interconnect sandwiched metal layers which were then measured at MIT \[56\]. Metal layers deposited with the tungsten sputtering rate a factor of 4 slower than the normal process showed no sheet resistance increase even after 5 hours at 550°C. This deposition modification to improve the WN\(_x\) barrier is a probable improvement to future
Vitesse processes and would extend the E-o-E integration technique time-temperature tolerance. An increased nitrogen concentration WN₄ layer was incorporated beneath the metal 4 bond-pad metal for the MIT-OEIC-3/NCIPT-OEVLSI-1 chip described in Sections 4.7 and 5.3 [58]. By reducing the WN₄ interdiffusion with the bond-pad AlCuₓ metal, improved post-thermal cycle wire bonding characteristics have been demonstrated (see Section 5.3). The interconnect metal thermal degradation currently determines the E-o-E growth sequence thermal constraint (e.g. 5 hours at \( \leq 470^\circ \)).

### 3.1.2 Ohmic Contacts and Resistors

Figure 3.3 shows the 5-hour-duration thermal cycle temperature response of the metal 1 - ohmic metal - S/D implant (M1-OM-N⁺) contact string resistance per contact, the metal 1 - ohmic metal (M1-OM) contact string resistance per contact...
3.1. ELECTRICAL DEVICES (THERMAL CHARACTERIZATION)

Figure 3.4: Ohmic contact resistance Arrhenius-based model (activation energy $\approx 2.5$ eV to $3.0$ eV) [56].

and the S/D implant sheet resistance. The M1-OM contact string via dimensions are identical to those in the M1-OM-N$^+$ contact string. In the 5-hour thermal cycle temperature range of 500$^\circ$C to 550$^\circ$C, the S/D implant sheet resistance and OM-M1 resistance per contact show no increase in resistance while the M1-OM-N$^+$ contact string resistance per contact increases by nearly two orders of magnitude. These observations clearly indicate that increased ohmic contact resistance is responsible for the increased M1-OM-N$^+$ resistance per contact.

All of the ohmic contact containing resistances exhibited common thermal cycle response features. The ohmic contact resistance increase was delayed in time, thermally activated ($E_a = 2.5$ eV to $3.0$ eV) and highly variable. Figure 3.4 shows the Arrhenius-based model curve set fitted to the measured ohmic contact resistances to predict the resistance for arbitrary thermal cycle times from 5 minutes to 1 week. The delay before the onset of ohmic contact resistance increase, however, was noted to correlate strongly with the ohmic contact metal 1 via spacing, defined as the distance
between the metal 1 via edge and the ohmic contact metal edge. This correlation is displayed Figure 3.5 and Table 3.1. Figure 3.5 shows the average measured MESFET source resistance and the small and large TLM structure resistances per unit contact length as a function of 5-hour thermal cycle temperature. The strong correlation between the ohmic contact to metal 1 via spacing and the 5-hour thermal cycle critical temperature is shown in Table 3.1. The 5-hour thermal cycle critical temperature was defined as the temperature where the resistance per unit contact length exceeded 2000 $\Omega - \mu m$.

This provides a basis for understanding the physical mechanism responsible for the ohmic contact resistance increase. It is proposed that the ohmic contact resistance increase is the result of a reaction between Al-Cu-W-N and Ni-Ge upon aluminum compound penetration through the $WN_x$ barrier to the ohmic contact metal edge. Strain due to thermal expansion mismatch between the ohmic metal and GaAs crystal is concentrated at the ohmic metal edge and is believed to provide a preferential site
### Table 3.1: Critical temperature and metal 1 via spacing for each ohmic contact structure shown in Figure 3.5 [57].

<table>
<thead>
<tr>
<th>Contact Type</th>
<th>Critical Temp. (°C)</th>
<th>Metal 1 Via Spacing (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small TLM</td>
<td>526</td>
<td>0.4</td>
</tr>
<tr>
<td>MESFET</td>
<td>529</td>
<td>0.5</td>
</tr>
<tr>
<td>Large TLM</td>
<td>547</td>
<td>2.0</td>
</tr>
</tbody>
</table>

![Diagram](image)

**Figure 3.6:** Ohmic contact cross sections as a function of time, read (a) to (d). Ohmic contact resistance increases substantially only when the Al-W-N compound reacts with the edge of the Ni-Ge (d) [56].
for new phase nucleation and growth [60]. Figure 3.6 is a schematic cross section of an ohmic contact at four times in a thermal cycle. The WN$_x$ barrier penetration to the ohmic metal edge (d1+d2) equals 2500 Å(d1) plus the via spacing (d2), thus explaining the correlation between ohmic contact to metal 1 via spacing (d2). It is believed that only when the Al-W-N compound reaches the strained Ni-Ge (i.e. at the edge of the contact) does new phase nucleation and growth of a high-resistivity compound occur.

To confirm the proposed physical mechanism underlying ohmic contact resistance degradation, as well as monitor electrical devices throughout the E-o-E sequence, several test structures were designed and fabricated on the MIT-OEIC-3 chip. These test structures are detailed in the MIT-OEIC-3 design and testing manual [58] as well as in Subsections 4.7.1 and 4.7.9. Table 3.2 summarizes the extracted parameters from test structures (cells) both before and after 5-hour thermal cycles at 470°C and 550°C. Thermal cycles were performed in an MBE reactor with the sample block temperature measured by infrared pyrometer. Extracted parameters include metal snake resistances (PCM 17, 19, 20, 22), contact string resistances (PCM 23, 25, 26, 28), TLM contact resistances (PCM 29-32), S/D implant resistances (PCM 18, 21), ohmic contact string resistances with a variety of contact geometries (EB 1-4) and ring oscillator frequencies (EB 5-6).

In agreement with the discussion in Subsection 3.1.1, the metal snakes and contact string resistances remained relatively constant before and after the 470°C thermal cycle, while the the resistances dramatically increased for the 550°C thermal cycle. These MBE thermal-cycle temperatures are accurate to within $\sim \pm 10^\circ$C with the uncertainty introduced by pyrometer fluctuations. TLM contact resistances and S/D implant resistances exhibit trends consistent with the ohmic contact degradation discussion. Of particular interest are contact strings with different via 1/ohmic metal geometries. From the correlations observed in thermal tests conducted on the standard Vitesse PCM, contacts with small metal 1 via spacings should have large
<table>
<thead>
<tr>
<th>Cell</th>
<th>Description</th>
<th>Before</th>
<th>After</th>
<th>Change</th>
<th>Before</th>
<th>After</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM 17</td>
<td>Gate metal resistor snake</td>
<td>1.56 kΩ</td>
<td>1.56 kΩ</td>
<td>+0.0</td>
<td>1.77 kΩ</td>
<td>1.78 kΩ</td>
<td>+0.6</td>
</tr>
<tr>
<td>PCM 19</td>
<td>Metal 1 resistor snake</td>
<td>35.7 kΩ</td>
<td>46.7 kΩ</td>
<td>+30.8</td>
<td>47.4 Ω</td>
<td>360 Ω</td>
<td>+655.3</td>
</tr>
<tr>
<td>PCM 20</td>
<td>Metal 2 resistor snake</td>
<td>16.0 Ω</td>
<td>20.1 Ω</td>
<td>+25.6</td>
<td>26.8 Ω</td>
<td>144 Ω</td>
<td>+437.3</td>
</tr>
<tr>
<td>PCM 22</td>
<td>Metal 3 resistor snake</td>
<td>3.67 Ω</td>
<td>6.05 Ω</td>
<td>+64.8</td>
<td>11.3 Ω</td>
<td>17.2 Ω</td>
<td>+52.5</td>
</tr>
<tr>
<td>PCM 23</td>
<td>Metal-1 / S/D implant contact string</td>
<td>56.3 kΩ</td>
<td>53.6 kΩ</td>
<td>-4.8</td>
<td>54.8 kΩ</td>
<td>&gt; 10 MΩ</td>
<td>+1000</td>
</tr>
<tr>
<td>PCM 24</td>
<td>Metal-1 / gate metal contact string</td>
<td>359 Ω</td>
<td>409 Ω</td>
<td>+13.9</td>
<td>390 Ω</td>
<td>655 Ω</td>
<td>+67.9</td>
</tr>
<tr>
<td>PCM 26</td>
<td>Metal-1 / metal-2 contact string</td>
<td>26.6 Ω</td>
<td>35.1 Ω</td>
<td>+32.0</td>
<td>33.2 Ω</td>
<td>199 Ω</td>
<td>+499.4</td>
</tr>
<tr>
<td>PCM 28</td>
<td>Metal-2 / metal-3 contact string</td>
<td>5.65 kΩ</td>
<td>8.77 Ω</td>
<td>+55.2</td>
<td>13.6 Ω</td>
<td>38.9 Ω</td>
<td>+186.0</td>
</tr>
<tr>
<td>PCM 29</td>
<td>TLM (100 μm wide, 5 μm gap)</td>
<td>18.3 Ω</td>
<td>21.1 Ω</td>
<td>+15.8</td>
<td>30.3 Ω</td>
<td>109.0 Ω</td>
<td>+259.7</td>
</tr>
<tr>
<td>PCM 30</td>
<td>TLM (100 μm wide, 10 μm gap)</td>
<td>30.7 Ω</td>
<td>35.0 Ω</td>
<td>+14.0</td>
<td>42.3 Ω</td>
<td>286.0 Ω</td>
<td>+576.1</td>
</tr>
<tr>
<td>PCM 31</td>
<td>TLM (100 μm wide, 5 μm gap w/ pass/describe cuts)</td>
<td>18.2 Ω</td>
<td>20.4 Ω</td>
<td>+12.1</td>
<td>31.8 Ω</td>
<td>150 Ω</td>
<td>+400</td>
</tr>
<tr>
<td>PCM 32</td>
<td>TLM (100 μm wide, 5 μm gap w/ pass/describe cuts)</td>
<td>30.7 Ω</td>
<td>32.7 Ω</td>
<td>+6.5</td>
<td>40.1 Ω</td>
<td>210 Ω</td>
<td>+423.7</td>
</tr>
<tr>
<td>PCM 33</td>
<td>S/D resistor (5 μm x 50 μm)</td>
<td>2.39 kΩ</td>
<td>2.39 kΩ</td>
<td>+0.0</td>
<td>2.41 kΩ</td>
<td>&gt; 10 MΩ</td>
<td>+1000</td>
</tr>
<tr>
<td>PCM 34</td>
<td>S/D resistor (20 μm x 5 μm)</td>
<td>88 Ω</td>
<td>92.1 Ω</td>
<td>+4.7</td>
<td>98.4 Ω</td>
<td>&gt; 10 MΩ</td>
<td>+1000</td>
</tr>
<tr>
<td>EB1</td>
<td>4 μm ohmic, 1.4 μm via metal-1 / S/D contact string</td>
<td>27.6 kΩ</td>
<td>28.4 kΩ</td>
<td>+2.9</td>
<td>28.3 kΩ</td>
<td>2.13 MΩ</td>
<td>+7.4 x 10^3</td>
</tr>
<tr>
<td></td>
<td>Per contact (304 contacts in string)</td>
<td>90.8 Ω</td>
<td>93.4 Ω</td>
<td>+2.9</td>
<td>93.1 Ω</td>
<td>7.0 kΩ</td>
<td>+7.4 x 10^3</td>
</tr>
<tr>
<td></td>
<td>Per contact x ohmic metal width</td>
<td>363.2 (Ω/c.) · μm</td>
<td>373.7 (Ω/c.) · μm</td>
<td>+2.2</td>
<td>372.4 (Ω/c.) · μm</td>
<td>26.0 KΩ</td>
<td>+7.4 x 10^3</td>
</tr>
<tr>
<td>EB2</td>
<td>4 μm ohmic, 3.0 μm via metal-1 / S/D contact string</td>
<td>27.4 kΩ</td>
<td>28.0 kΩ</td>
<td>+2.2</td>
<td>27.9 kΩ</td>
<td>5.19 MΩ</td>
<td>+18.5 x 10^3</td>
</tr>
<tr>
<td></td>
<td>Per contact (304 contacts in string)</td>
<td>90.1 Ω</td>
<td>92.1 Ω</td>
<td>+2.2</td>
<td>91.8 Ω</td>
<td>17.1 kΩ</td>
<td>+18.5 x 10^3</td>
</tr>
<tr>
<td></td>
<td>Per contact x ohmic metal width</td>
<td>360.5 (Ω/c.) · μm</td>
<td>368.4 (Ω/c.) · μm</td>
<td>+2.2</td>
<td>367.1 (Ω/c.) · μm</td>
<td>68.3 KΩ</td>
<td>+18.5 x 10^3</td>
</tr>
<tr>
<td>EB3</td>
<td>2 μm ohmic, 1.4 μm via metal-1 / S/D contact string</td>
<td>48.0 kΩ</td>
<td>49.5 kΩ</td>
<td>+3.1</td>
<td>49.0 kΩ</td>
<td>52.2 MΩ</td>
<td>+106.4 x 10^3</td>
</tr>
<tr>
<td></td>
<td>Per contact (304 contacts in string)</td>
<td>157.9 Ω</td>
<td>162.8 Ω</td>
<td>+3.1</td>
<td>161.2 Ω</td>
<td>171.7 kΩ</td>
<td>+106.4 x 10^3</td>
</tr>
<tr>
<td></td>
<td>Per contact x ohmic metal width</td>
<td>315.8 (Ω/c.) · μm</td>
<td>325.7 (Ω/c.) · μm</td>
<td>+3.1</td>
<td>322.4 (Ω/c.) · μm</td>
<td>343.4 KΩ</td>
<td>+106.4 x 10^3</td>
</tr>
<tr>
<td>EB4</td>
<td>Metal 1 - gate metal - ohmic metal - S/D contact string</td>
<td>69.5 kΩ</td>
<td>82.3 kΩ</td>
<td>+18.4</td>
<td>71.5 kΩ</td>
<td>142.0 kΩ</td>
<td>+0.099 x 10^3</td>
</tr>
<tr>
<td></td>
<td>Per contact (304 contacts in string)</td>
<td>228.6 Ω</td>
<td>270.7 Ω</td>
<td>+18.4</td>
<td>232.5 Ω</td>
<td>467.1 kΩ</td>
<td>+0.099 x 10^3</td>
</tr>
<tr>
<td></td>
<td>Per contact x ohmic metal width</td>
<td>548.7 (Ω/c.) · μm</td>
<td>649.7 (Ω/c.) · μm</td>
<td>+18.4</td>
<td>654.5 (Ω/c.) · μm</td>
<td>1.12 Ω</td>
<td>+0.099 x 10^3</td>
</tr>
<tr>
<td>EB5</td>
<td>23 stage ring osc.</td>
<td>4.2 ns per</td>
<td>4.4 ns per</td>
<td>+4.8</td>
<td>3.0 ns per</td>
<td>failed</td>
<td>failed</td>
</tr>
<tr>
<td></td>
<td>91 ps/stg.</td>
<td>96 ps/stg.</td>
<td>96 ps/stg.</td>
<td>+4.8</td>
<td>65 ps/stg.</td>
<td>failed</td>
<td>failed</td>
</tr>
<tr>
<td>EB6</td>
<td>23 stage ring osc. w/o M1-ohmic contact</td>
<td>4.2 ns per</td>
<td>4.6 ns per</td>
<td>+9.5</td>
<td>3.0 ns per</td>
<td>5.0 ns per</td>
<td>+66.6</td>
</tr>
<tr>
<td></td>
<td>91 ps/stg.</td>
<td>100 ps/stg.</td>
<td>100 ps/stg.</td>
<td>+9.5</td>
<td>65 ps/stg.</td>
<td>100 ps/stg.</td>
<td>+66.6</td>
</tr>
</tbody>
</table>
resistance increases (see Table 3.1) after 5-hour thermal cycles at around 550°C (see Figure 3.5). To isolate the effects of the the metal 1 via spacing, previously defined as the distance between the edge of via 1 and the edge of the ohmic contact metal, three contact strings were designed. Contact string EB1 has a 4.0 μm × 4.0 μm ohmic metal pad with a centered 1.4 μm × 1.4 μm metal 1 via, EB2 has a 4.0 μm × 4.0 μm ohmic metal pad with a centered 3.0 μm × 3.0 μm metal 1 via and EB3 has a 2.0 μm × 2.0 μm ohmic metal pad with a centered 1.4 μm × 1.4 μm metal 1 via. All contact strings have 304 contacts. (The ring oscillator results, EB5-6, will be discussed in the next subsection.)

As shown in Table 3.2, the PCM EB1-3 series of test structures exhibits the expected thermal degradation trend. The EB 1-3 metal 1 via spacings are 1.3 μm, 0.5 μm and 0.3 μm, respectively, and the change in resistance per contact is +7.4×10^3%, +18.5×10^3% and +106.4×10^3%, respectively, after a 5-hour thermal cycle at 550°C. These data clearly show that the onset and extent of ohmic contact degradation is determined by the metal 1 via spacing. A fourth contact string, EB4, was designed and tested to serve as a control. If the ohmic contact degradation mechanism is a reaction between Al-Cu-W-N and Ni-Ge upon aluminum compound penetration through the WN_x barrier to the ohmic contact metal edge, then a contact string without a direct metal 1 to ohmic metal contact should not exhibit the same characteristic resistance increase. The EB4 has a 2.4 μm × 2.4 μm ohmic metal pad with no metal 1 via directly to the ohmic metal. EB4 instead has ohmic metal running to a pad of gate metal which is contacted by a 1.4 μm × 1.4 μm metal 1 via. Table 3.2 shows that EB4 has a higher resistance per contact before thermal cycle, due to the added resistance of the gate metal runner, but that the increase is only 0.099×10^3% after a 5-hour thermal cycle at 550°C. This increase is approximately two orders of magnitude lower than the best direct metal 1 via to ohmic metal, EB1, and clearly indicates that the degradation mechanism is different. EB4 resistance increase is presumably due to the degradation of the individual metal lines. In addition to serving as an experimental
control, EB4 suggests an alternate contact scheme if higher thermal cycle (i.e. MBE growth temperature) stability is required. Increased metal 1 via spacing can also be beneficial.

### 3.1.3 Enhancement and Depletion MESFETs

Measurements of 5 EFETs and 3 DFETs of varying gate width and length were performed before and after each thermal cycle. The Schottky gate contact was stable for all thermal cycles with $\phi_b$ and $n$ showing no significant trends. However, MESFET transconductances and saturation currents decreased as the source and drain resistances increased. Figure 3.7 shows the $R_S$, $g_m$ and $I_{DS}$ for these FETs as a function of maximum thermal cycle temperature, ranging from 400°C to 600 °C. Figure 3.7 demonstrates that the FET characteristics are stable for 5 hours at temperatures up to approximately 525°C. This is consistent with the ohmic contact resistance increase which begins at approximately 525°C (see Figure 3.5). Figure 3.8 plots the threshold voltage of a 10 $\mu$m $\times$ 1.0 $\mu$m EFET, a representative device, as a function of the 5-hour thermal cycle temperature. $V_T$ increases slightly up to approximately 520°C and then drops dramatically. Following severe thermal cycles, such as 5 hours at 550°C, the MESFET source resistance measurements over 9 devices showed coefficient of variation ($\sigma$/mean) approaching unity in addition to large average increase. The statistical spread in ohmic contact resistance increase is believed to be the result of the nonuniform penetration of aluminum through the WN$_x$ barrier [59]. MESFET HSPICE device simulations showed that the transconductance and saturation current decreases were accurately modeled by including resistors at the MESFET source and drain terminals equal to the measured source and drain resistance increases.

Considering the increase in metal 1 - 3 sheet resistances, which begins at approximately 475°C, and the increase in ohmic contact resistance, which begins at approximately 525°C, which occurs after 5-hour thermal cycles, E-o-E optoelectronic integration optical device growth must be performed at 475°C or less. To confirm
Figure 3.7: Vitesse HGaAs3 E-MESFET and D-MESFET source resistance, transconductance and source-drain current for a variety of FET geometries for 5-hour thermal cycles with maximum temperatures between 400°C and 600°C [56].
Figure 3.8: Threshold voltage, $V_T$, shifts for $10 \mu m \times 1.0 \mu m$ Vitesse HGaAs3 E-MESFETs after 5-hour thermal cycles with maximum temperatures between 400°C and 600°C [56].

that there are negligible MESFET characteristic shifts after 5-hour thermal cycles at a temperature of 475°C, EFETs and DFETs were examined under these conditions. Figure 3.9 and Figure 3.10 plot $10 \mu m \times 1.0 \mu m$ EFET and $10 \mu m \times 1.0 \mu m$ DFET characteristics, respectively, after 5-hour thermal cycles at 475°C. Figure 3.9 shows that EFET $I_{DS-V_{DS}}$, $g_m$ and $R_S$ curves are virtually identical before and after the thermal cycles. Figure 3.10 shows the same stability trends as observed for the EFET as well as virtually identical Schottky barrier heights and idealities before and after thermal cycles.

In addition to individual device characteristics, the E-o-E growth sequence must also preserve the high uniformity inherent in the commercial VLSI GaAs MESFET circuitry. Electronics uniformity is especially critical for large optoelectronic array applications [6]. To verify that high FET uniformity is maintained through thermal cycles, 13 pairs of FETs were designed and fabricated across the MIT-OEIC-3 chip.
Figure 3.9: 10.0 μm × 1.0 μm Vitesse HGaAs3 E-MESFET before and after a 5-hour 475°C thermal cycle. In side view, the panels are as follows: upper left shows $I_{DS}$ vs. $V_{DS}$, upper right shows $I_{DS}$ vs. $V_{GS}$ and lower left shows $V_{DS}$ vs. $I_{GS}$ [56].
Figure 3.10: 10.0 μm × 1.0 μm Vitesse HGAs3 D-MESFET before and after a 5-hour 475°C thermal cycle. In side view, the panels are as follows: upper left shows $I_{DS}$ vs. $V_{DS}$, upper right shows $I_{DS}$ vs. $V_{GS}$, lower left shows $V_{DS}$ vs. $I_{GS}$ and lower right shows $I_{GS}$ vs. $V_{GS}$ [56].
The placement of each pair is shown in Section 4.7, Figure 4.44. Each FET pair is representative of a typical DCFL inverter ($\beta \approx 7$) with a 10 $\mu$m $\times$ 1.2 $\mu$m EFET and a 3.4 $\mu$m $\times$ 2.8 $\mu$m DFET. Table 3.3 summarizes the FET characteristics both before and after a 5-hour, 470°C thermal cycle. The far right column shows the change in the percent deviation from before to after the thermal cycle. Vitesse cross-wafer threshold voltages and standard deviations are typically $V_T$ mean = 0.277 V and $\sigma$ = 0.020 V for 10 $\mu$m $\times$ 0.6 $\mu$m EFETs and $V_T$ mean = -0.679 V and $\sigma$ = 0.041 V for 10 $\mu$m $\times$ 0.6 $\mu$m DFETs [28]. Though the devices are sized differently and the cross-chip spread is expected to be smaller than the cross-wafer spread, the $V_T$ mean = 0.334 and $\sigma$ = 0.016 V for 10 $\mu$m $\times$ 1.2 $\mu$m EFETs and $V_T$ = -0.712 V and $\sigma$ = 0.021 V for 3.4 $\mu$m $\times$ 2.8 $\mu$m DFETs after a 5 hour, 470°C thermal cycle compares favorably with variations reported by Vitesse. This level of uniformity is extremely difficult to achieve with noncommercially fabricated electronics, which demonstrates another merit of the E-o-E optoelectronic integration technique.

The mean percentage shifts of $E g_m$ and $D V_T$ on this chip, from before to after the 5-hour thermal cycle at 470°C, were larger than expected based on 5-hour thermal cycles conducted in the range of 400°C to 600°C [56]. While the mean percentage shifts of $E V_T$ (+1.8%), $E I_{DS}$ (-1.7%), $D g_m$ (-1.5%) and $D I_{DS}$ (-0.02%) were minimal, the $E g_m$ (-25.5%) and $D V_T$ (-13.0%) mean shifts were large. Large changes in $\sigma\%$ also occur for $E g_m$ (8.9% to 2.9%) and $D V_T$ (6.0% to 2.9%) which suggests a possible explanation. Thermal cycles in this temperature range are often observed to tighten the statistical spread. The mean of the spread can shift, while $\sigma$ decreases, if there is a preferred shift direction. Small-area (e.g. chip size) uniformity studies may be susceptible to this phenomenon, due to local process variations, while large area (e.g. wafer size) uniformity studies would tend to average this effect. An extensive thermal cycle uniformity study is clearly warranted.

A simple measure of generic circuit performance, as a function of optical device growth temperature, is indicated by the oscillation period of a ring oscillator. As
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Table 3.3: E_{MESFET} (10.0 μm x 1.2 μm) and D_{MESFET} (3.4 μm x 2.8 μm) after a 5-hour, 47°C thermal cycle.
shown in Figure 3.11, the oscillation period of 23-stage DCFL ring oscillators was unaffected by thermal cycling after 5 hours at up to 450°C. Following 5 hours at 450°C to 540°C, the ring oscillator period was measured to increase by about 10%, but remained well within the delay distribution before cycling. However, no oscillations were observed after 5-hour thermal cycles at 550°C and above. HSPICE simulations, including the ohmic contact resistances at the MESFET source and drain terminals, correctly predicted that ring oscillators would not function after 5-hour thermal cycles above 540°C. To confirm that the ring oscillator failure is primarily due to ohmic contact resistance increase, thus reducing voltage swing at the output of each inverter stage in the ring until the oscillator fails, a ring oscillator was designed and fabricated without the use of metal 1 - ohmic metal contacts. Referring once again to Table 3.2, the ring oscillator with standard metal 1 - ohmic metal contacts (EB5) failed after a 5-hour thermal cycle at 550°C while a ring oscillator (EB6) with the contact scheme used in EB4 continued to ring after the thermal cycle. There was a significant slow down
in the oscillator frequency, presumably due to the same mechanism which increases the resistance per contact in the EB4 test structure.

In summary, E-o-E optical device growth should be performed at temperatures below 475°C in 5 hours or less. Some tradeoff between time and temperature is possible as suggested by the Arrhenius-based model plots. All electrical device parameters, including electrical interconnect resistances, ohmic contact resistances, EFETs, DFETs, Schottky diodes, uniformity and ring-oscillator frequencies are well behaved for 5-hour thermal cycles at temperatures as high as 470°C.

3.1.4 Resonant-Tunneling Diodes

In addition to electrical devices fabricated in the Vitesse GaAs E/D MESFET process, electrical devices may also be epitaxially grown in the dielectric growth wells. While both optical and electrical devices can be grown and fabricated in a single DGW
at the same time, by stacking the epilayers and selective processing, many circuits require only one or the other. A high-speed, low-power static random access memory (SRAM) cell is an example of a circuit which benefits from using the E-o-E integration technique to fabricate quantum electronic devices in the DGWs.

An SRAM cell based on commercial EFETs and two resonant-tunneling diodes (RTDs) has recently been proposed by R.J. Aggarwal (Fonstad's group at MIT) [61]. Important RTD figures of merit for optimal SRAM performance (e.g. high-speed and low static power) are a low resonance voltage, a sharp turn-on current and a large peak-to-valley-current ratio (PCVR). To achieve these characteristics, RTDs are frequently grown with high indium concentration materials lattice matched to InP (see Figure 2.12). Alternatively, a strain-relieved buffer can be grown on GaAs thereby changing the substrate lattice constant to match that of the high indium concentration In$_x$Ga$_{1-x}$As RTD layers. An In$_{0.22}$Ga$_{0.78}$As/AlAs relaxed-buffer RTD with a PCVR of 13:1 has been recently demonstrated using two layers in the relaxed buffer, each beyond critical thickness [62]. An I-V characteristic of an In$_{0.27}$Ga$_{0.73}$As/AlAs relaxed-buffer RTD is shown in Figure 3.12 [61]. The relaxed buffer for this RTD consisted of 0.2 μm In$_{0.11}$Ga$_{0.89}$As and 0.2 μm In$_{0.27}$Ga$_{0.73}$As, both doped n$^+$. 

As seen in Figure 3.12, the resonance voltage is ~ 0.9 V, the turn-on current is sharp and the PCVR is ~ 3.75. In addition, the voltage drop across the relaxed-buffer is typically ≤ 30 mV [63]. These characteristics are well suited for integration with DCFL MESFET circuitry. Relaxed-buffer RTDs can be grown within the E-o-E thermal constraints and, based on these initial results, RTD-based SRAM cells and an array have been designed and fabricated on the MIT-OEIC-3 chip. Design details are presented in the MIT-OEIC-3 design and testing manual (SRAM sections written by R.J. Aggarwal) [58] and in Subsection 4.7.6.
3.2 Optical Detectors

Optical detectors allow optical signals to be converted to electrical signals. These electrical signals are processed with the VLSI GaAs MESFET circuitry and ultimately determine the emission or modulation of subsequent optical signals. This section presents four optical detectors compatible with the E-o-E optoelectronic integration technique. The first two, optical enhancement-mode MESFET detectors (Subsection 3.2.1) and $\lambda \leq 0.87 \, \mu\text{m}$ sensitive metal-semiconductor-metal detectors (Subsection 3.2.2), can be fabricated with standard Vitesse process steps. These detectors are particularly attractive because they do not require an epitaxial growth sequence. Receiver circuits can, therefore, be fabricated without a growth sequence, while a single growth sequence yields optoelectronic circuits with both emitters/modulators and detectors; no epitaxial stacking or complex processing is needed. For special applications such as long-wavelength sensitivity or tunable wavelength detectors, however, the epitaxial growth sequence can be devoted to a detector heterostructure. Two such epitaxial detectors are $\lambda \leq 1.30 \, \mu\text{m}$ metal-semiconductor-metal detectors (Subsection 3.2.3) and multiple-quantum-well p-i-n detectors (Subsection 3.2.4). Each of these four photodetectors is well suited for certain applications. Other optical detectors are compatible with the E-o-E technique, such as long wavelength ($\sim 10 \, \mu\text{m}$) quantum well intersubband photodetectors (QWIPs). Preliminary low-temperature (77 K) measurements of Vitesse MESFETs have shown that devices are functional (e.g. $\sim 50\%$ $g_m$ increase) at temperatures compatible with QWIP operation [52]. QWIPs and other E-o-E compatible photodetectors are being developed.

3.2.1 Optical Enhancement MESFET

An enhancement-mode MESFET, fabricated in the standard Vitesse process, can serve as a high-gain, low-frequency optical detector. Light incident on the channel area modulates the channel potential, thereby controlling the drain-source current.
Figure 3.13: Schematic illustration of an OPFET structure fabricated in the standard Vitesse process.

By increasing the space between the gate and the source/drain contacts the optical MESFET (OPFET) geometry is better matched to optical beam spot sizes. With the gate terminal floating, dark currents of tens of nanoamperes and responsivities as high as 2000 A/W are possible for wavelengths around 830 nm. Ion-implanted MESFET OPFETs have been studied in recent years [64, 65, 66, 67, 68] and the mechanisms responsible for MESFET photosensitivity were found to be primarily traps in the substrate, photoconductivity and the photovoltaic effect if the substrate or gate terminal potentials are not fixed. OPFETs fabricated with the standard Vitesse process have been extensively studied by our collaborator, Dr. Annette C. Grot (formerly of Psaltis’ group at Caltech) [69], and the results are detailed in her Ph.D. thesis [70]. Mechanisms and models specific to Vitesse OPFETs will be overviewed in this subsection.

Figure 3.13 shows the structure of an OPFET fabricated at Vitesse. An enhancement-
mode MESFET is fabricated in a geometry compatible with an optical beam spot size, typically from 5 to 20 \( \mu \text{m} \) in diameter. An OPFET with a 1.0 \( \mu \text{m} \) gate length, 40 \( \mu \text{m} \) gate width and a gate-source and gate-drain spacing of 10 \( \mu \text{m} \) is depicted. Most of the 10 \( \mu \text{m} \times 40 \mu \text{m} \) area on either side of the gate, formed by pulling the drain and source away from the gate, is S/D n\(^+\) implanted. Only approximately 0.8 \( \mu \text{m} \) on either side of the gate, which is protected by spacer oxide, and the area under the gate is not S/D implanted. The area under the spacer eventually receives an n (silicon) implant dose which is higher than the enhancement dose \(-\) and lower than the S/D dose. Therefore, most of the optical absorption occurs in the shallow (\( \sim 0.1 \mu \text{m} \)) S/D implant region and the deeper (\( \sim 1.0 \mu \text{m} \)) p\(^-\) implant between the gate and the source/drain. Recall that the p\(^-\) layer was produced by Vitesse implants which improve uniformity by doping the substrate at a density higher than the mid-band gap trap density present in the starting GaAs substrate (liquid encapsulated Czochralski grown).

Figure 3.14 shows the \( I_{DS}-V_{DS} \) characteristics for a typical OPFET with various incident optical powers. These characteristics are strikingly similar to the family of curves produced by varying the gate potential on an enhancement-mode MESFET. In fact, as Figure 3.15 illustrates, there is an exact correspondence between applied gate voltages and incident optical powers. In the case shown, a \( V_g = 0.4 \) V and an incident optical power of 270 nW produce nearly identical \( I_{DS}-V_{DS} \) curves. It is, therefore, reasonable to expect the light to be controlling the channel potential just as the electrical bias does on the Schottky-barrier gate.

Figure 3.16 is a log-log plot of \( I_{DS} \) vs. incident optical power both before and after a 5-hour, 530\(^\circ\)C thermal cycle (e.g. optical device growth sequence). The decrease in responsivity after thermal cycling is believed to be due to an increased voltage drop across the ohmic source/drain contacts, which reduces the intrinsic \( V_{DS} \).

Figure 3.17 shows the responsivity as a function of incident optical power wavelength. The responsivity begins to drop at approximately 825 nm and falls to nearly
CHAPTER 3. DEVICES FOR E-O-E OEICS

Figure 3.14: I-V characteristics of an enhancement-mode FET with different light intensities illuminating the gate region (L=2.8μm, W=13.6μm). The optical source was an AlGaAs/GaAs laser diode operating at 840 nm. The responsivity of this device at 10 nW is determined to be 1800 A/W [71].

Figure 3.15: Similarity between optical and electrical control over drain-source current on an OPFET [70].
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Figure 3.16: Efficiency of OPFET before and after thermal cycle (e.g. LED growth). $V_{DS} = 1.0 \text{ V}$ and the gate was left floating [70].

Figure 3.17: OPFET responsivity as a function of incident optical power wavelength [72].
zero around the Ge:As band gap, \( \sim 870 \) nm.

A model for the Vitesse OPFETs has been proposed by A.C. Grot [70] and model parameters were extracted for use in simulations. The channel region of an OPFET (enhancement-mode MESFET) is n-type and is contacted from above by the Schottky-barrier gate and from below by the p\(^{-}\) implant layer. The resulting electron energy band diagram has an energy valley, with a minimum electron potential characterized by \( \Phi_s \), which is the difference between the conduction band minimum and the Fermi-level. For gate biases above threshold there is a conducting channel (i.e. \( \Phi_s \) small). For gate biases below threshold the channel region is totally depleted (i.e. \( \Phi_s \) large) and there should be no drain-source current. However, subthreshold diffusion currents still flow according to

\[
I_{DS} = I_o e^{\frac{-Q\Phi_s}{kT}} e^{\frac{-Q\Delta V_g}{kT}} \left( 1 - e^{\frac{Q\Phi_s}{kT}} \right)
\]

(3.5)

\( I_o \) is a geometry dependent constant and \( \kappa \) is a coefficient which represents the fraction of \( \Delta V_g \) which appears across the channel region, thereby producing \( \Delta \Phi_s \) (\( \Delta \Phi_s = -\kappa V_g \)). The coefficient \( \kappa \) deviates from unity because the gate-channel capacitance \( (C_{GC}) \) is in series with the channel-p\(^{-}\)-layer substrate/backgate capacitance \( (C_{CB}) \) as expressed by

\[
\frac{1}{\kappa} = 1 + \frac{C_{GC}}{C_{CB}}
\]

(3.6)

Typical Vitesse OPFET \( \kappa \) values range from 0.5 to 0.7 [70].

When a positive electrical bias is applied to the gate terminal of an E-MESFET, a positive voltage appears across the gate-channel junction which reduces \( \Phi_s \). Similarly, when an optical signal is incident on an OPFET, a positive voltage appears across the channel-substrate junction due to the photovoltaic effect in this n-p junction. This positive voltage reduces \( \Phi_s \) which lowers the electron diffusion barrier and increases subthreshold current. Because the p\(^{-}\) layer substrate/backgate is not contacted, the
3.2. **OPTICAL DETECTORS**

channel-substrate voltage is the open-circuit photovoltaic voltage given by

\[
V_{OC} = \frac{kT}{q} \ln \left( \frac{P_{in}}{P_{th}} \right) \quad \text{for} \quad P_{in} >> P_{th}
\]  

(3.7)

where \( P_{in} \) is the incident optical power and \( P_{th} \) is the thermal generation rate in the channel region.

From this discussion it is clear that the \( p^- \) layer is acting as a photo-modulated backgate terminal. Under optically controlled backgate operation, \( V_{OC} \) in Equation 3.7 is analogous to \( V_G \) for electrically controlled "topgate" operation. As the incident optical signal power is increased, \( V_{OC} \) increases which causes \( \Phi_S \) to decrease resulting in an increase in \( I_{DS} \). For maximum responsivity operation the gate terminal is left floating which allows that gate voltage to follow the substrate potential, thus enhancing the channel from both sides. Alternatively, by controlling the gate potential the minimum channel potential can be altered, thereby changing the responsivity of the OPFET. A convenient way to model OPFET operation is to simply equate E-MESFET gate voltages with OPFET incident optical powers across the \( I_{DS} - V_{DS} \) characteristics. Standard MESFET models can then be used with the additional relationship between optical power and gate voltage. Experimental measurements yield the following relationship:

\[
V_G = \frac{kT}{q} \ln \left( \frac{P_{in} \eta_o}{I_o} \right)
\]  

(3.8)

\( P_{in} \) is expressed in units of watts, \( \eta_o \approx 340 \text{ A/W} \) and \( I_o \approx 20 \text{ nA} \).

This model correctly predicts the characteristics of the OPFET, but not transients. This model limitation is a consequence of using an E-MESFET HSPICE model, with an optical power to gate voltage conversion relation, but not including \( C_{CB} \) photocarrier charging dynamics. The frequency response can be measured experimentally and used in conjunction with the modeling technique to design optical receivers. The time response of OPFET detectors was measured by Grot [70] by applying a square wave optical pulse to the OPFET and measuring \( I_{DS} \). The gate was left floating and
Figure 3.18: Output voltage of a current amplifier fed by the response of an optical E-MESFET to a small optical pulse (40 nW) [70].

Figure 3.19: Output voltage of a current amplifier fed by the response of an E-MESFET to an applied electrical pulse (0.4 V) [70].
the \( I_{DS} \) was fed into a current amplifier (741 op-amp, \( 2V/\mu s \) slew rate, \( R_{\text{feedback}} = 4.6 \) k\( \Omega \)). Figure 3.18 shows the op-amp output voltage waveform for a 40 nW incident optical square wave. Rise and fall times are approximately 25 \( \mu s \), which are much faster than the long fall times typical of deep traps present at the surface of recess-etched OPFETs [73]. The time response is believed to be determined by the RC time constant associated with the photogenerated carrier charging of the channel-p\textsuperscript{-} substrate/backgate capacitor. Figure 3.19 shows the op-amp output voltage waveform, under identical conditions to Figure 3.18, except that a 0.4 V electrical square wave signal was applied to the OPFET gate instead of an optical signal. This confirmed that the test setup was not frequency limiting the measurement.

### 3.2.2 Metal-Semiconductor-Metal (\( \lambda \leq 0.87 \mu m \))

Metal-semiconductor-metal (MSM) photodetectors can also be fabricated with the standard Vitesse process steps. MSM photodetectors are typically high speed and have no gain. MSM detectors consist of two sets of interdigitated metal fingers forming Schottky-barrier contacts to the underlying semiconductor crystal. The metal finger widths and spacings are optimized to yield maximum light collection efficiency (typically narrow fingers) and maximum responsivity (typically large electric fields between closely spaced fingers). A Vitesse MSM optical detector is schematically shown in Figure 3.20 where gate metal is patterned to produce the metal fingers. Ideally, when a bias is applied between the two sets of fingers the semiconductor is fully depleted between the fingers. This electric field in the depleted semiconductor sweeps out photogenerated electron-hole pairs to produce a current at the terminals. Semi-insulating GaAs can be fully depleted with low external bias.

In the standard Vitesse process flow all active areas receive at least an enhancement-mode MESFET ion-implantation. To deplete the regions between the metal fingers a higher external bias must be applied for implanted material. An additional mask step could be used to protect the MSM detector regions from the ion implantation.
Unfortunately this modification is currently exclusively licensed to IBM by Vitesse [31] and is, therefore, unaccessible through MOSIS.

Vitesse MSM detectors still have excellent performance even with this undesirable enhancement-mode silicon implant. Sheu et al. [74] have built several high speed receivers based on Vitesse HGaAs2 MSM photodetectors and E/D MESFET transimpedance amplifiers in the past four years. A typical MSM consists of seven 1.2-μm-wide fingers with 1.6 μm spacings covering a total area of 20 × 20 μm². This structure had low parasitic capacitance (0.1 - 0.2 pF), low dark current (< 100 nA), good quantum efficiency (35 - 40%) and reasonable sensitivity (0.27 - 0.37 A/W). In conjunction with a monolithic transimpedance amplifier containing six MESFETs, two Schottky diodes and one feedback resistor (tunable D-MESFET), a data rate of 1 Gb/s, noise of 3.8 pA/Hz¹/², sensitivity of <-28 dBm and dynamic range > 30 dB was achieved. The MSM detector required a ± 5 V bias, standard DCFL rail voltages (0,-2 V) and the entire receiver circuit occupied 224 μm × 72 μm while consuming
3.2. OPTICAL DETECTORS

Figure 3.21: Spectral response of Vitesse MSM photodetector and MSM-transimpedance amplifier pair. The MSM detector sensitivity was normalized to unity at 750 nm (Norm. MSM Sensitivity). The MSM detector sensitivity was further corrected (Norm. MSM Sensitivity Corrected for Source Power) for the black body source power curve (Norm. Source Power) which was also normalized to unity at 750 nm. The MSM with T.I. Amp. curve shows expected DCFL output voltages as the input wavelength is swept from high absorption wavelengths ($\leq$ 870 nm) to low absorption wavelengths. Roll-off frequencies are indicated with dashed vertical lines.

roughly 500 mW of power. Superior performance should be possible with the Vitesse HGaAs3 technology, since it has lower minimum feature sizes, and with alternate transimpedance circuit designs. Regardless, this demonstrates that MSM detectors available in the standard Vitesse process are well suited for high-speed applications.

MSM detectors with transimpedance (T.I.) amplifiers were designed, in collaboration with Peter Nuytken [75], and fabricated in this work. The spectral responses of the MSM detector and the MSM-T.I. amplifier pair are shown in Figure 3.21. The MSM detector sensitivity was normalized to unity at 750 nm (Norm. MSM Sensitiv-
ity). The MSM detector sensitivity was further corrected (Norm. MSM Sensitivity Corrected for Source Power) for the black-body optical-source power curve (Norm. Source Power) which was also normalized to unity at 750 nm. For these measurements the MSM detector bias was maintained at 5.0 V. The MSM with T.I. Amp. curve shows the expected DCFL output voltages as the input wavelength is swept from high absorption wavelengths (≤ 870 nm) to low absorption wavelengths. For these measurements, standard DCFL rail voltages were maintained (0,-2 V) while the D-MESFET feedback resistor gate voltage was maintained at -2.33 V. These circuits will be detailed in Sections 4.6 and 4.7.

3.2.3 Metal-Semiconductor-Metal (λ ≥ 0.87 μm)

Thus far only optical detectors fabricated with standard Vitesse process steps have been described. The detectors presented in this subsection and the next require an epitaxial growth step. An optical detector, very similar in structure to the MSM presented in the last subsection, but sensitive to wavelengths of 1.30 μm and beyond can be fabricated. As discussed in Section 2.4, all epitaxial devices must be grown within the time-temperature budget of 5 hours at 470°C as well as be lattice matched to the underlying GaAs. Figure 3.22 depicts a heterostructure grown in a DGW and an MSM detector fabricated on the upper epitaxial layers. While such a growth is routine for GaAs/AlGaAs materials, these materials have low optical absorption below the GaAs band gap (∼ 0.87 μm). Narrower band gap materials such as In₀.₄Ga₀.₆As are required for optical sensitivity at the important optical fiber wavelength of 1.30 μm. Though In₀.₄Ga₀.₆As is a highly lattice mismatched material on GaAs, if a thick step-graded structure is grown, defects are trapped below the top device layers. This idea was previously discussed in Section 3.1.4 and was exploited to fabricate high peak-to-valley ratio RTDs.

A typical heterostructure, as demonstrated by Sacks et al. [76] is as follows (from substrate up): 0.5 μm In₀.₂Ga₀.₈As, 0.5 - 1.0 μm In₀.₄Ga₀.₆As, 500 ÅIn₀.₄(Ga,Al)₀.₆As
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Figure 3.22: Strained-layer MSM photodiode fabricated in a dielectric growth well.

with graded Ga and Al, and finally 100 Å In$_{0.4}$Al$_{0.6}$As. A GaAs buffer can be grown below this to bring the total heterostructure thickness to 4.2 μm, which aligns the top layer with the DGW sidewall. The lattice mismatched layers were designed to minimize dislocations in the optically active layer and near carrier-collection electrodes. High Schottky-barrier MSM fingers were achieved with Ti/Pt/Au metallization on a lattice matched, graded In$_{0.4}$(Ga,Al)$_{0.6}$As cap layer. Dark currents were typically < 400 nA at 20 V and the carrier collection efficiency was ~ 90%. The MSM responsivity at 25 V applied bias was 0.39 A/W for a detector with a 0.5 μm In$_{0.4}$Ga$_{0.6}$As layer while a 1.0-μm-thick layer yielded 0.48 A/W sensitivity. Devices with 2.0 μm finger spacings exhibited a 3 dB bandwidth of 4.5 GHz [76]. These results, combined with E-o-E integration technique compatible growth conditions, suggest that high speed 1.30-μm-sensitive MSM photodetectors are achievable with the E-o-E technique. DGWs with associated transimpedance amplifiers have been designed for this purpose. Subsection 4.7.2 will detail this E-o-E optoelectronic circuit.
3.2.4  Multiple-Quantum-Well p-i-n

Another epitaxially grown optical detector compatible with the E-o-E integration technique is the p-i-n photodiode. Figure 3.23 shows a p-i-n epitaxial structure which consists of a n⁺ GaAs buffer on the bottom, an n AlGaAs barrier, an intrinsic GaAs absorption layer and a p AlGaAs layer on the top. The absorption layer is typically \( \sim 1 \mu m \) thick and absorbs nearly all incident photons. Applying a reverse bias to the diode structure creates an electric field in the absorption layer and sweeps the photogenerated carriers to the contact terminals.

The optical absorption spectrum can be designed by using various materials and structures in the absorption layer. Multiple quantum wells (MQWs) can be included to either raise or lower the band edge absorption. InGaAs/GaAs quantum wells can be used to extend the maximum absorption wavelength beyond 1.0 \( \mu m \) while AlGaAs layers or AlGaAs quantum wells can decrease the minimum absorption wavelength
3.2. OPTICAL DETECTORS

<table>
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<th>3E18</th>
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<th>GaAs</th>
<th>Contact</th>
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<td>Spacer</td>
<td></td>
</tr>
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<td>n+</td>
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<td>25A</td>
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</table>

Figure 3.24: GaAs/AlGaAs MQW p-i-n photodiode heterostructure compatible with the E-o-E optoelectronic integration technique. This layer structure can also be used to fabricate MQW modulators and SEED devices [72].

down to the visible spectrum. An (Al,Ga)As p-i-n heterostructure compatible with the E-o-E optoelectronic integration technique is shown in Figure 3.24.

MQW modulators and self-electrooptic effect devices (SEEDs) can also be fabricated from this heterostructure as detailed in Section 3.3.4. The total layer thickness is 4.2 μm which aligns the top layer with the DGW sidewall top surface. The distributed Bragg reflector (DBR) layers form a mirror which reflects normal incidence light back through the MQW absorbing layers, thereby increasing the detector efficiency. DBR spectral characteristics will be presented in Section 3.4.2. Optical absorption occurs primarily in the not-intentionally-doped (NID) 70 period GaAs/Al0.30Ga0.70As MQW region. The MQW region is sandwiched between a p+ GaAs top contact layer and the n+ lower DBR layers, thereby forming the p-i-n structure.

The layer structure shown in Figure 3.24 was designed by our collaborator Jiafu Luo (Psaltis’ group at Caltech) [72] and was grown at MIT [77] under conditions
Figure 3.25: P-i-n detector photocurrent as a function of reverse applied bias. The epitaxial layers are given in Figure 3.24.

very nearly compatible with E-o-E integration constrains (e.g. 500°C growth temperature, instead of 470°C, for 5 hours). Detectors were fabricated and characterized at Caltech. Figure 3.25 is a plot of the responsivity vs. wavelength of a p-i-n photodetector fabricated from the epitaxial layers presented in Figure 3.24. The MQW region exhibits excitonic resonances which enhance absorption at specific wavelengths. Consistent with the quantum confined Stark effect (QCSE) [78], the excitonic peaks are red shifted by an applied electric field. The electron-heavy hole (ehh) resonance is at a lower energy (longer wavelength) than the electron-light hole (e lh) and the ehh peak is red shifted by approximately 7 nm with a reverse bias of -8 V. Responsivities are typically \( \sim 0.5 \text{ A/W} \) at the ehh peak wavelength. These values are typical of MQW p-i-n heterostructures. High-speed and transient characteristics of these devices remains to be measured.
3.3 \textbf{Optical Emitters}

Optical emitters are devices which convert electrical signals to optical signals. Together with optical detectors, discussed in the previous subsection, complete optical interconnect links can be built. In the next section, Section 3.4, optical modulators will be presented which can often be used instead of optical emitters. This section will present four optical emitters, each particularly well suited for certain applications. Light-emitting diodes (LEDs) are incoherent optical sources and will be discussed in Subsection 3.3.1. LEDs are ideal for extremely low power applications, since they do not have a threshold current. Subsection 3.3.2 will cover in-plane (in the plane of the chip) laser diodes which are typically used for emitting high single-mode powers into in-plane waveguide or fibers. In-plane surface-emitting lasers (IPSELs) are described in Subsection 3.3.3 and are similar to in-plane laser diodes except that mirrors are etched into the crystal near the laser facets to redirect the optical emission vertically. Surface-normal emission is essential for two-dimensional optoelectronic array applications. Finally, Subsection 3.3.4 describes a vertical-cavity surface-emitting laser (VCSEL) structure compatible with the E-o-E integration technique. Until recently, VCSELs required very thick epitaxial growths typically at high temperatures for several hours. In addition, the threshold voltages were quite high. All of these issues, which historically prevented VCSEL structures from being compatible with the E-o-E technique, have been addressed in the past five years and VCSELs are now well positioned for use in E-o-E OEICs.

3.3.1 \textbf{Light-Emitting Diodes}

Light-emitting diodes (LEDs) are commonly grown by sandwiching a lower energy gap, lightly doped active region between higher energy gap, n- and p-doped barriers. This forms a p-i-n diode double heterostructure which can be processed into a device that efficiently converts injected carriers into photons when forward biased. LEDs are
designed to maximize this conversion efficiency. In addition, LEDs must be designed to efficiently extract these photons from the device. This is particularly challenging because incoherent light is emitted in all directions and is predominantly reflected by the large index step between (Al,Ga)As and air. This subsection will address these issues and present experimental LED results.

LED wall-plug efficiency ($\eta$) is defined as the ratio of the optical output power ($P_{out}$) to electrical input power ($P_{in}$) and is an important figure of merit for optical emitters. Wall-plug efficiency benefits from a high electron-to-photon conversion efficiency ($\eta_s$) as well as good photon extraction efficiency. Electron-to-photon conversion efficiency depends heavily on the minority carrier lifetime ($\tau$), which is typically the electron lifetime for lightly p-type materials. The value of $\tau$ depends on the radiative recombination lifetime ($\tau_r$), the nonradiative recombination lifetime ($\tau_{nr}$) and the interfacial recombination “lifetime” ($w/2s$) as expressed by

$$\frac{1}{\tau} = \frac{1}{\tau_r} + \frac{1}{\tau_{nr}} + \frac{2s}{w}. \quad (3.9)$$

High $\eta_s$, and therefore high $\eta$, requires $\tau$ to approach $\tau_r$, which in turn requires a low $\tau_r$, a high $\tau_{nr}$, a large $w$ (active region width) and a small $s$. In this subsection, calculations will first be presented to quantify the photon conversion efficiency trends.

A proposed heterostructure, based on the calculated design curves and compatible with the E-o-E optoelectronic integration technique, is then described and experimental results are presented. Finally, photon extraction techniques are briefly discussed. The discussion in this section is based on the review of low-current LED design by Lin [79] and is extended to include the constraints imposed by the E-o-E integration technique.

To calculate $\eta_s$, the minority carrier distribution in the LED active region must be determined. A lightly doped p-type GaAs active region will be assumed and justified later. The minority carrier (electron) conduction current can be approximated under
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low-level injection conditions as

\[ J_n = q\mu_n n E + qD_n \frac{dn}{dx} \approx qD_n \frac{dn}{dx} \quad (3.10) \]

The minority continuity equation which relates the minority current, the total minority carrier generation rate \( (G_n) \), the minority carrier recombination rate \( (R_n) \) and the temporal rate of change of the minority carrier concentration \( (dn/dt) \) is expressed as

\[ \frac{dn}{dt} = G_n - R_n + \frac{1}{q} \frac{dJ_n}{dx} \quad (3.11) \]

Under steady state conditions \( (dn/dt = 0) \) and without external generation \( (G_{ext} = 0) \), Equation 3.11 simplifies to

\[ g_{th} - R_n + \frac{1}{q} \frac{dJ_n}{dx} \approx -\frac{\Delta n}{\tau_n} + \frac{1}{q} \frac{dJ_n}{dx} = \nu \quad (3.12) \]

where \( g_{th} \) is the thermal generation rate and \( g_{th} - R_n \) has been approximated as the excess electron density \( (\Delta n) \) divided by the electron lifetime given in Equation 3.9. Substitution of Equation 3.10 into Equation 3.12 yields

\[ \frac{d^2 \Delta n}{dx^2} - \frac{\Delta n}{L_n^2} = 0 \quad \left( L_n = \sqrt{D_n \tau_n} \right) \quad (3.13) \]

where \( L_n \) is the electron diffusion length. The boundary conditions for this second order differential equation are

\[ \frac{d\Delta n}{dx}(x = 0^+) = \frac{J}{qD_n} - \frac{s\Delta n(x = 0^+)}{D_n} \quad (3.14) \]

\[ \frac{d\Delta n}{dx}(x = w^-) = -\frac{s\Delta n(x = w^-)}{D_n} \quad (3.15) \]

where the interfacial recombination velocity, \( s \), [80] for GaAs/AlGaAs interfaces is
approximated as [81]

\[
s \approx 2 \times 10^7 \cdot \frac{\Delta a}{a} \approx 2000 \frac{cm}{s}
\]  

(3.16)

where \( \Delta a/a \) is the relative lattice constant mismatch at the interface. Solving for \( n(x) \) yields

\[
\Delta n(x) = \frac{J L_n}{q D_n} \frac{\cosh \left( \frac{w-x}{L_n} \right) + s \frac{L_n}{D_n} \sinh \left( \frac{w-x}{L_n} \right)}{\left( \left( \frac{s L_n}{D_n} \right)^2 + 1 \right) \sinh \left( \frac{w}{L_n} \right) + 2 \frac{s L_n}{D_n} \cosh \left( \frac{w}{L_n} \right)}
\]  

(3.17)

\( P_{out} \) can now be calculated by integrating the product of the photon generation rate \( (\eta(x)/\tau_r) \) and the self-absorption \( (e^{-\alpha(w-x)}) \) over the width of the active region as follows:

\[
P_{out} = A \frac{hc}{\lambda} \int_0^w \frac{\Delta n(x)e^{-\alpha(w-x)}}{\tau_r} dx
\]

\[
= \frac{\tau}{\tau_r \eta_s \frac{hc}{q \lambda} I}
\]  

(3.18)

where \( A \) is the LED lateral area, \( \lambda \) is the emission wavelength and \( \eta_s \) is expressed as

\[
\eta_s = \frac{\frac{1+S}{1-\alpha L_n} \left[ 1 - e^{-\alpha \left( \frac{1-\alpha L_n}{L_n} \right) e^{\frac{w}{L_n}} - \frac{1-S}{1+\alpha L_n} \left[ 1 - e^{\alpha \left( \frac{1+\alpha L_n}{L_n} \right) e^{\frac{w}{L_n}}} \right] \right]}{2 \left( (S^2 + 1) \sinh \left( \frac{w}{L_n} \right) + (2S) \cosh \left( \frac{w}{L_n} \right) \right) e^{\alpha w}}
\]  

(3.19)

with

\[
S = s \frac{L_n}{D_n}
\]  

(3.20)

For simplicity the emission and absorption spectra is treated only at a single wavelength, \( \lambda \).

A few observations regarding \( P_{out} \) maximization are now appropriate. First, \( \tau/\tau_r \) should be nearly unity in order for most injected electrons to recombine and radiate photons. Therefore, referring to Equation 3.9, \( s \) should be minimized and \( \tau_{nr} \) should be maximized. This can be achieved by decreasing \( \Delta a/a \) (e.g. decrease the aluminum mole fraction, \( x \), in Al\(_x\)Ga\(_{1-x}\)As and grow high-quality heterointerfaces) to reduce \( s \) and by decreasing the active layer doping concentration to increase \( \tau_{nr} \). Auger
3.3. **OPTICAL EMITTERS**

recombination, which is nonradiative, increases with increasing carrier concentration. Second, \( \eta_s \) should be large. This requires the active layer width \( (w) \) to be optimized. Since \( \eta_s \) increases with increasing \( w \) for \( \alpha \approx 0 \) and finite \( s \), there is reason to make \( w \) large. However, since \( \eta_s \) decreases with increasing \( w \) for finite \( \alpha \) and \( s \approx 0 \), there is reason to make \( w \) small. These cases are extreme limits and realistic heterostructures will have finite \( \alpha \) and \( s \) terms. Self-consistent calculations are required to optimize \( w \) and therefore \( \eta_s \). A final observation, regarding \( P_{out} \) maximization, is that the overall radiative recombination should be maximized. There are three ways to do this: 1) increase the carrier confinement, and therefore the electron-hole overlap, by increasing the barrier heights by keeping \( \tau \) high in the \( \text{Al}_x\text{Ga}_{1-x}\text{As-GaAs-Al}_x\text{Ga}_{1-x}\text{As} \) heterostructure, 2) increase the total photon emission by keeping \( w \) large since \( P_{out} \propto \int_0^w G_{\text{photon}} R_{\text{photon}} dw \), 3) decrease \( \tau_r \), while keeping \( \tau_{nr} \) large, by doping the active region and increasing the injected current density since \( \tau_r \propto 1/p \) where \( p \) is the free-hole concentration (this dependency will be derived shortly). Thus there are some obvious tradeoffs that must be taken into account and optimized in designing a high-efficiency LED structure.

Before self-consistently calculating \( n(x) \), \( \eta_s \) and \( P_{out} \), an expression for the minority carrier (electron) radiative lifetime is required. From the theory of bimolecular recombination [82], the spontaneous band-to-band recombination rate, \( R_{sp} \), is given by

\[
R_{sp} = B np
\]  
(3.21)

where \( B \) is the radiative recombination probability and is approximately \( 1 \times 10^{-10} \) cm\(^3\)/s for GaAs [83]. With current injection, \( R_{sp} \) becomes

\[
R_{sp} = B \left( n_o + \Delta n \right) \left( p_o + \Delta p \right)
\]  
(3.22)

With \( \Delta n = \Delta p \)

\[
R_{sp} = B n_o p_o + B \Delta n \left( p_o + n_o + \Delta n \right)
\]  
(3.23)
For at least minimally p-type GaAs (e.g. \(N_A \geq 1 \times 10^{14} \text{ cm}^{-3}\)) the terms in Equation 3.23 involving \(n_o\) can be neglected. \(R_{sp}\) can, therefore, be simplified to

\[
R_{sp} = B \Delta n (N_A + \Delta n)
\]  
(3.24)

The radiative recombination lifetime is defined as

\[
\tau_r \equiv \frac{\Delta n}{R_{sp}}
\]  
(3.25)

and thus, after substituting Equation 3.24 into Equation 3.25, the radiative lifetime can be expressed as

\[
\tau_r = \frac{1}{B(N_A + \Delta n)}
\]  
(3.26)

Equation 3.26 states that the radiative recombination lifetime is inversely proportional to the sum of the acceptor doping concentration, assuming fully ionized acceptors, and the injected electron concentration, i.e. the free-hole concentration.

The last relation needed before self-consistently calculating LED design curves is \(\tau_r\) as a function of the injected current density, \(J\), instead of \(\Delta n\). \(J/nq\) is equal to the total recombination per unit area in the active region which is equal to the total excess population (\(\Delta n \times w\)) divided by the lifetime (\(\tau_n\)). Since the current is predominantly electron current, \(\Delta n\) can be solved to yield the desired expression:

\[
\Delta n = \frac{J\tau_n}{nq} = \frac{J\eta_{int}\tau_r}{nq}
\]  
(3.27)

where \(\eta_{int}\) is the internal quantum efficiency (set to unity for simplicity in these calculations). Equation 3.27 can now be substituted into Equation 3.26, resulting in the quadratic expression for \(\tau_r\)

\[
\tau_r = \frac{1}{B(N_A + \Delta n)} = \frac{1}{B(N_A + \frac{J\eta_{int}\tau_r}{nq})}
\]  
(3.28)
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<table>
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<th>$\tau_{nr}$ increased by:</th>
<th>$s$ decreased by:</th>
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<td>Narrow active region ($\propto e^{-\omega w}$)</td>
<td>Low defect count</td>
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<tr>
<td>Doped active region ($\propto 1/N_A$)</td>
<td>Low doping (Auger)</td>
<td>Lattice matching ($\propto \Delta a/a$)</td>
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<tr>
<td>High level injection ($\propto 1/\Delta n$)</td>
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<td>Low surface recomb.</td>
</tr>
<tr>
<td>Carrier confinement ($\propto \int e, h \text{ overlap}$)</td>
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</tr>
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</table>

Table 3.4: Photon conversion efficiency trends.

which can, finally, be solved for the radiative recombination lifetime:

$$
\tau_r = \frac{qw \left( -N_A + \sqrt{N_A^2 + \frac{4J}{q\omega B}} \right)}{2J}
$$

(3.29)

The LED efficiency trends are summarized in Table 3.4.

The following pages contain design curves for LED heterostructures based on the preceding discussion. There are several design parameters to optimize and precise values for many of the parameters are unknown. Also, the limitations of the lowered growth temperature, and therefore an upper limit on the Al mole fraction in the AlGaAs barriers as well as possibly compromised AlGaAs/GaAs interface quality, must be taken into account. To address all of these issues, the following design curves have been plotted over a wide range of operating conditions (e.g. injected current densities) as well as loss and interfacial recombination velocity.

Three figures are plotted to demonstrate the dependency of the radiative recombination lifetime, $\tau_r$, on the active layer thickness, $w$, the injected current density, $J$, and the active layer doping concentration, $N_A$. First, Figure 3.26 shows $\tau_r$ plotted as a function $w$, for various values of $J$. $N_A$ is fixed at $1 \times 10^{16}$ cm$^{-3}$ which is a typical active region doping concentration. Next, Figure 3.27 shows $\tau_r$ plotted as a function of $N_A$ for various $J$. The value of $w$ is fixed at 0.60 $\mu$m, which is a typical active region width. Finally, Figure 3.28 shows $\tau_r$ plotted as a function of $J$ for various $N_A$. Again, $w$ is fixed at 0.60 $\mu$m. Together these plots demonstrate that a low radiative lifetime is achieved through a combination of low active layer thickness, high active
region doping concentration and high injected current density.

The next two figures consider the dependence of the electron-photon conversion efficiency, $\eta_s$, on the interface recombination velocity, $s$, and GaAs absorption coefficient, $\alpha$. Figure 3.29 shows $\eta_s$ plotted as a function of $w$ for various values of $s$. $\alpha$ is fixed at $0$ cm$^{-1}$, $J = 100$ A/cm$^2$ and $N_A = 1 \times 10^{16}$ cm$^{-3}$ for this plot. While these values of $J$ and $N_A$ are typical, $\alpha$ is artificially set to 0 for demonstration purposes only. Figure 3.30 shows $\eta_s$ plotted as a function of $w$ for various values of $\alpha$. $s$, is fixed at $0$ cm/s, $J = 100$ A/cm$^2$ and $N_A = 1 \times 10^{16}$ cm$^{-3}$. Once again, while these values of $J$ and $N_A$ are typical, $s$ is artificially set to 0 for demonstration purposes only. These figures clearly indicate that extremely wide active regions are desirable in the limit of no self-absorption by the active region. On the other hand, extremely narrow active regions yield the highest electron-photon conversion efficiencies if the interfacial recombination velocity is negligible.

The last three figures simultaneously treat finite $\alpha$ and $s$. All three plots assume an active region doping concentration of $1 \times 10^{16}$ 1/cm$^3$ p-type. This value is high enough to contribute to maintaining a low $\tau_r$ under low-level current injection, yet is low enough to not substantially decrease $\tau_{nr}$ via Auger recombination. All three plots, Figures 3.31, 3.32 and 3.33, show $\eta_s$ vs. $w$ but for injected current densities of 10 A/cm$^2$, 100 A/cm$^2$ and 1000 A/cm$^2$, respectively. All three figures plot 9 combinations of $\alpha$ and $s$ values ranging from $\alpha = 10^{3.5}$ to $10^{4.5}$ and $s = 10^2$ to 104. From these figures it is clear that to select an active area width, not only must $\alpha$ and $s$ be estimated, but the operating current density for a particular application must be known.

Focusing attention on Figure 3.32, which assumes a $J = 100$ A/cm$^2$ which corresponds to $\sim 0.6$ mA for a $25 \times 25$ $\mu$m$^2$ area and is therefore typical of currents per LED in a large array, various $\eta_s$ are seen. For $\alpha = 10^4$ and $s = 10^3$, which are typical for GaAs/AlGaAs heterostructures, an optimal active region width is 0.6 $\mu$m. This is a reasonable width because it is positioned such that small $\alpha$ and $s$ deviations
from the assumed values \( n_s \) will not cause large shifts in \( \eta_s \). An LED heterostructure designed from these calculations will now be described.
Figure 3.26: Radiative recombination lifetime, $\tau_r$, plotted as a function of active layer thickness, $w$, for various injected current densities, $J$. The active layer doping concentration, $N_A$, is fixed at $1 \times 10^{16} \text{ cm}^{-3}$.

Figure 3.27: Radiative recombination lifetime, $\tau_r$, plotted as a function of active layer doping concentration, $N_A$, for various injected current densities, $J$. The active layer width, $w$, is fixed at 0.60 $\mu\text{m}$.
Figure 3.28: Radiative recombination lifetime, $\tau_r$, plotted as a function of injected current density, $J$, for various active layer doping concentrations, $N_A$. The active layer width, $w$, is fixed at 0.60 $\mu$m.

Figure 3.29: LED electron-photon conversion efficiency, $\eta_s$, plotted as a function of active layer thickness, $w$, for various interface recombination velocities, $s$. The absorption coefficient, $\alpha$, is fixed at 0 cm$^{-1}$, $J = 100$ A/cm$^2$ and $N_A = 1 \times 10^{16}$ cm$^{-3}$. 
Figure 3.30: LED electron-photon conversion efficiency, $\eta_e$, plotted as a function of active layer thickness, $w$, for various absorption coefficients, $\alpha$. The interface recombination velocity, $s$, is fixed at 0 cm/s, $J = 100$ A/cm$^2$ and $N_A = 1 \times 10^{16}$ cm$^{-3}$.

Figure 3.31: LED electron-photon conversion efficiency, $\eta_e$, plotted as a function of active layer thickness, $w$, for various absorption coefficients, $\alpha$, and interface recombination velocities, $s$. $J = 10$ A/cm$^2$ and $N_A = 1 \times 10^{16}$ cm$^{-3}$.
Figure 3.32: LED electron-photon conversion efficiency, $\eta_e$, plotted as a function of active layer thickness, $w$, for various absorption coefficients, $\alpha$, and interface recombination velocities, $s$. $J = 100$ A/cm$^2$ and $N_A = 1 \times 10^{16}$ cm$^{-3}$.

Figure 3.33: LED electron-photon conversion efficiency, $\eta_e$, plotted as a function of active layer thickness, $w$, for various absorption coefficients, $\alpha$, and interface recombination velocities, $s$. $J = 1000$ A/cm$^2$ and $N_A = 1 \times 10^{16}$ cm$^{-3}$. 
CHAPTER 3. DEVICES FOR E-O-E OEICS

Figure 3.34 presents four possible LED heterostructures suggested by the preceding calculations. Figure 3.34 (a) is the simplest heterostructure and has a 6000 Å, $1 \times 10^{16}$ p-type active region. 6000 Å allows for possibly increased $s$ due to lowered temperature MBE growth which can result in rough hetero-interfaces. The p-type doping is important for low injected current density operation. A 3000 ÅAl$_{0.3}$Ga$_{0.7}$, $1 \times 10^{18}$ n-type barrier bounds the active region from below and a 7000 ÅAl$_{0.3}$Ga$_{0.7}$As, $1 \times 10^{18}$ p-type barrier bounds the active region from above. The Al concentration is kept low to reduce the effects of oxygen incorporation in the AlGaAs which is a concern when grown at lowered temperatures. The upper barrier is thicker than the lower barrier to allow for better current distribution. The top most layer is a 1000 ÅGaAs, $5 \times 10^{18}$ contact layer. Finally, the lowest layers are a GaAs/AlGaAs (or InGaAs/GaAs), $3 \times 10^{18}$ n-type superlattice to impede defect propagation from the surface and a 2.5 μm GaAs, $3 \times 10^{18}$ spacer layer to bring the total device thickness to 4.2 μm to match the top surface of the DGW, which is important for integration processing. This structure, and a few variations, have been experimentally measured and the results will be presented after briefly describing the other structures in Figure 3.34.

Figure 3.34 (b) is identical to (a) except that the Al$_{0.3}$Ga$_{0.7}$As layers have been replaced by Al$_{0.4}$Ga$_{0.6}$Ga layers. The precise Al concentration is less important than the trend that it represents. Specifically, as improved lowered-temperature growth techniques are employed it is expected that increasing Al concentrations can be used without increased $s$. InGaP/GaAs LEDs can also be designed without concern for large $s$ since optimal growth temperatures are within the thermal constraints set by the E-o-E technique. Figure 3.34 (c) and (d) include DBR stacks below the active region to reflect the emitted light back towards the surface [79]. The benefits of a DBR will be discussed along with other photon extraction techniques. Both (c) and (d) have slightly thinner active regions which indicates that high quality interfaces, and therefore low $s$, is required for DBR growth and the active region should make
use of this fact. (d) also includes a quarter-wave stack on top which serves as a semiconductor antireflection (AR) layer. AR coatings will also be discussed with various processing techniques which can improve photon extraction and, therefore, wall-plug efficiency.

The LED heterostructure shown in Figure 3.34 (a) was grown at the lowered growth temperature of 530°C \(^1\). The epitaxial layers were wet-chemical etched (1:1:6 \(\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{Acetic acid}\)) to form current confining mesas. A thin electrically insulating dielectric layer (\(\text{SiO}_2\)) was deposited followed by a via etch (buffered oxide etch) and p-type metallization (\(\text{AuZn/Au}\)). Back-side n-type contact was formed by evaporating \(\text{AuGe/Ni/Au}\) and annealing the entire structure (\(\sim 400^\circ\text{C}\) for \(\sim 15\) sec.). A detailed LED process flow is shown in Appendix A. The LED I-V characteristic is shown in Figure 3.35 and the LED L-I characteristic is shown in Figure 3.36. The threshold voltage is \(\sim 1.2\) V. The efficiencies obtained were low (0.01% at 100\(\mu\)A and 0.03% at 1 mA) presumably due to the lack of current confinement, except for the etched mesas. To explore this hypothesis, similar LEDs were grown at 700° and were identically processed to serve as a growth-temperature control sample [69]. LEDs fabricated in this high-temperature material had nearly identical I-V curves and equally low efficiencies, supporting the idea that the low efficiencies were inherent in the heterostructure design or processing as opposed to the lowered-temperature growth material quality.

There are several ways to improve the wall-plug efficiency of these LEDs. The electron-to-photon conversion efficiency can be improved by using higher energy barriers and thinner active regions. Such modifications require high quality material which can be achieved by using advanced low-temperature growth techniques or by using \((\text{In,Ga})\text{AsP}\) rather than \((\text{Al,Ga})\text{As}\) (i.e. a material system which is optimally grown at 470° or below, see Section 2.5). An \((\text{In,Ga})\text{AsP}\) LED heterostructure, iden-

\(^{1}\) Historically 530°C was an important growth temperature because ohmic contacts do not degrade significantly and conventional MBE techniques produce decent AlGaAs material at this growth temperature. Future LEDs will be grown at 470°C in the \((\text{In,Ga})\text{AsP}\) material system.
Figure 3.34: Various LED heterostructures. (c) and (d) are based on structures found in [79].
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Figure 3.35: LED I-V characteristic for heterostructure in Figure 3.34 (a) [71].

Figure 3.36: LED L-I characteristic for heterostructure in Figure 3.34 (a) [71].
tical to Figure 3.34 (a) expect that the AlGaAs was replaced by GaAs lattice matched (In,Ga)P (In$_{0.49}$Ga$_{0.51}$P), was grown at 470°C by J.A. Ahadian at MIT [47]. Simple LEDs were fabricated by shadow evaporating 500-μm-diameter ohmic contact pads. Efficiencies of $\sim 3 \times 10^{-4}$ W/A were typical and were roughly four times larger than similar AlGaAs based LEDs which were identically processed [90]. This demonstrates a significant efficiency increase which should scale to smaller and more sophisticated LED structures.

The value of $\eta_s$ can also be improved by increasing the injected current density and decreasing mesa sidewall recombination. High resistance ion-implantations (e.g. proton implants) and double Zn diffusions (not compatible with E-o-E technique) can be used to channel current to the center of a mesa structure, thereby increasing the current density and separating the current from the sidewalls [6]. An order of magnitude efficiency increase can be expected with ion-implanted current confinement [69]. A recently developed AlAs oxide can also be used to create a current aperture. This technique will be discussed in association with VCSELs in Subsection 3.3.4.

However, these improvements do not address the primary LED wall-plug efficiency limitation which is photon extraction. The large refractive index difference between GaAs and air results in a small critical angle ($\Theta_{crit}$), beyond which photons suffer total internal reflection. $\Theta_{crit} = 16.7^\circ$ for photons escaping from GaAs into air, which limits the LED wall-plug efficiency to roughly 2% (i.e. $S(16.7)^\circ/S(360)^\circ = 0.021$) even for unity electron-to-photon conversion. The 2% efficiency assumes that emission is collected from only one of the six sides of the LED cube. Roughly 2% efficiency is expected from all sides, which suggests possible collection techniques. To compound the problem, photons which would otherwise escape, by being within the escape cone, are partially reflected by the GaAs/air interface ($R_\perp = 32\%$) and absorbed by the ohmic contacts. Clearly these limitations must be addressed for efficient operation of optoelectronic circuits such as large two-dimensional arrays.

A method to dramatically improve photon extraction from LED structures, which
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involves roughening the top epitaxial surface, has recently been reported [84, 85].
The key to increasing photon extraction is to give the photons multiple opportunities
to find the escape cone. A textured top surface elastically scatters the photons and
thereby randomizes the photon propagation direction. One possible way to texture
a surface is to coat the surface with a randomly close-packed array of polystyrene
spheres (e.g. 0.2 μm in diameter) and then using these spheres as a dry etch mask. By
etching ~0.2 μm deep, external efficiencies of 30% have been demonstrated [84]. This
demonstration also included a DBR stack beneath the LED active region, thereby
nominally doubling the emission through the top facet, and injecting current nearly
laterally between the two ohmic contacts to minimize absorption at the contacts. Such
surface roughening methods, DBR stacks and current channeling are compatible with
the E-o-E technique.

Even without surface texturing wall-plug efficiencies can be increased. Possibilities include AR coating the top surface, using a transparent ohmic contact metal
(e.g. indium-tin oxide, ITO) and fabricating angled mirrors around the perimeter of
the LED to collect and redirect side emission. Such angled mirrors can be fabricated
by dry etching the crystal, by angle etching the dielectric sidewall and depositing
a reflective coating or by surrounding the LED with interconnect metal vias to ap-
proximate an angled metal surface. The last two methods are unique to the E-o-E
integration technique and should be a simple addition to the standard E-o-E process
flow. High-efficiency LEDs should be possible with a combination of these methods.

3.3.2 In-Plane Lasers

In-plane laser diodes are similar to LEDs except that mirrors, forming an optical
cavity, are essential and one or more quantum wells form the active region. These
quantum wells confine the injected carriers, while a core layer and cladding layers,
which are etched to form a longitudinal ridge, create a single lateral-mode optical
cavity. In-plane laser diodes are typically high speed and are capable of launching
hundreds of milliwatts of optical power into single-mode optical fibers. Laser diode optimization for use in E-o-E integration must also consider the effects of decreased AlGaAs layer quality as the growth temperature is reduced (see Section 2.5).

An AlGaAs/GaAs laser diode heterostructure, with a single InGaAs strained-layer active region, was grown by molecular beam epitaxy (MBE) at the lowered substrate temperature of 530°C. The heterostructure was designed by building on previously reported reduced-temperature laser diodes [38, 39] and low-threshold single-quantum-well (SQW) 980 nm lasers fabricated with an etch-stop layer [86]. The design objective was to fabricate a laser diode (4 μm ridge width and a 500 μm cavity length) which could be grown in under 5 hours at 530°C or less. Threshold currents should be below 100 mA (compatible with MESFET drive circuits) and threshold voltages should be less than 2.0 V (compatible with DCFL rail voltages). While such a device would not necessarily be optimal, it would demonstrate a laser diode with geometries and drive characteristics compatible with E-o-E integration. While a growth temperature of 530°C would degrade the standard interconnect metallization, the ohmic contacts and intrinsic devices would survive and thus, 530°C was set as an initial target growth temperature.

The SQW separate confinement laser heterostructure consists of an undoped 6 nm In_{0.2}Ga_{0.8}As active layer [87, 88, 89] sandwiched between two undoped 200 nm GaAs waveguiding layers as shown in Figure 3.37. These layers are centered between two 1.4 μm Al_{0.22}Ga_{0.78}As cladding layers (Si doped 5 × 10^{18} cm^{-3} n-type on bottom and Be-doped 1 × 10^{18} cm^{-3} on top). To further reduce the effects of nonradiative recombination centers in the lowered-temperature AlGaAs, the Al mole fraction is even lower and the waveguiding layers are even wider than those previously reported. A 3 nm AlAs etch-stop layer in the p-type Al_{0.22}Ga_{0.78}As cladding layer positioned 140 nm above the GaAs waveguiding layer (for single-mode operation), a 100 nm p^{+} (1 × 10^{19} cm^{-3}) GaAs layer above the p-type Al_{0.22}Ga_{0.78}As and a 10 nm p^{+}

\footnote{Increased nitrogen concentration interconnect lines should withstand growth sequences at 530°C.}
In$_{0.3}$Ga$_{0.7}$As top contact layer were also included. The entire structure was grown by conventional MBE techniques, as opposed to more complex techniques sometimes used for low-temperature growth [39, 41, 44], on Si-doped GaAs (100) substrates with a 0.5 μm n GaAs buffer layer. Two samples were grown with different growth temperature profiles, as shown in Figure 3.37. For sample A the In$_{0.2}$Ga$_{0.8}$As active layer and the GaAs waveguiding layer were grown at 530°C (pyrometer), while the Al$_{0.22}$Ga$_{0.78}$As cladding layers were grown at 600°C. For sample B the entire structure was grown at 530°C. A moderate group V/III flux ratio of roughly 3 was maintained throughout growth.

Laser diodes were fabricated by selective wet chemical etching the 4-μm-wide ridge structure using a succinic acid solution [86]. Silicon nitride was deposited and etched to expose the p$^+$ In$_{0.3}$Ga$_{0.7}$As contact layer on the ridge. Ti-Pt-Au p-type and Au-Ge-Ni-Au n-type metallization completed the process.

All devices operated continuous wave (cw) at room temperature with similar L-I
Table 3.5: Comparison of performance characteristics for sample A: Al$_{0.22}$Ga$_{0.78}$As grown at 600°C and sample B: Al$_{0.22}$Ga$_{0.78}$As grown at 530°C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sample A</th>
<th>Sample B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1000 µm</td>
<td>446 µm</td>
</tr>
<tr>
<td>$I_{th}$</td>
<td>29.7 mA</td>
<td>36.7 mA</td>
</tr>
<tr>
<td>$J_{th}$</td>
<td>0.743 kA/cm$^2$</td>
<td>2.06 kA/cm$^2$</td>
</tr>
<tr>
<td>$V_{th}$</td>
<td>1.51 V</td>
<td>1.72 V</td>
</tr>
<tr>
<td>Lasing $\lambda$</td>
<td>991 nm</td>
<td>987 nm @ 80 mA</td>
</tr>
</tbody>
</table>

characteristics. As summarized in Table 3.5, sample A had average threshold currents of 29.7 mA (0.74 kA/cm$^2$) and 36.7 mA (2.06 kA/cm$^2$) for 1000-µm and 446-µm-long devices, respectively, while sample B had average threshold currents of 72.0 mA (1.80 kA/cm$^2$) and 82.0 mA (4.10 kA/cm$^2$) for 1000-µm and 500-µm-long devices, respectively. Threshold voltages ranged from 1.5 V to 2.0 V and the lasing wavelengths were close to 980 nm, in agreement with photoluminescence measurements.

The devices grown at 530°C, sample B, operated cw and have performance within the initial bounds set for integration. Their threshold current density is, however, 2 to 2.5 times larger than that of the devices with AlGaAs cladding layers grown at 600°C, sample A, under otherwise identical conditions. This implies that there is additional absorption and/or nonradiative recombination in the cladding layers grown at 530°C which is affecting the laser diode performance.

While further AlGaAs laser diode optimization is almost certainly possible, InGaP/GaAs laser diodes are optimally growth around 470°C and are, therefore, a natural candidate for laser diodes. In-plane laser diodes with threshold currents ≤72 A/cm$^2$ and a growth temperature below 500°C have recently been reported [45]. While similar performance may be possible in the (In,Ga,Al)As material system with complex low-temperature growth techniques, (In,Ga)AsP based laser diodes are conventionally and simply grown at these low temperatures. For this reason, recent work has been focused on growing and processing (In,Ga)AsP laser diodes under conditions
compatible with E-o-E integration. Preliminary in-house work by J.A. Ahadian (Fonstad's and Kolodziejski's groups at MIT) has produced broad-area lasers with threshold current densities below 200 A/cm² [90]. The layer structure is identical to that shown in Figure 3.37 except that the AlGaAs layers were replaced by In₀.₄₉Ga₀.₅₁P layers. Future LEDs and in-plane laser diodes, for use with E-o-E OEICs at MIT, will primarily be (In,Ga)AsP based.

3.3.3 In-Plane Surface-Emitting Lasers

For many applications laser emission normal to the substrate plane is desired. So-called surface-emitting lasers are divided into two categories depending on how the optical beam comes to be directed normal to the substrate plane. In-plane surface-emitting lasers (IPSELs) are conventional in-plane lasers, as discussed in the previous subsection, and have vertical cavity mirrors and deflecting mirrors etched in the crystal to redirect the emission. Vertical-cavity surface-emitting lasers (VCSELs) operate quite differently. An active (gain) region is sandwiched between two very high reflectivity, epitaxial DBR stacks and optical oscillation occurs in the growth direction (e.g. in the Z direction if the X-Y plane contains the epitaxial layers). Each SEL structure has distinct advantages and disadvantages, and it is clear that an optoelectronic integration technique should be capable of integrating both classes of SEL. High-power, high external differential quantum efficiency (ηₐ) applications often require IPSELs, while high-density two-dimensional arrays often benefit from the small VCSEL footprint. This subsection will discuss IPSEL fabrication which was conducted in collaboration with Dr. William D. Goodhue, Dr. Joe P. Donnelly and G.D. Johnson of MIT Lincoln Laboratory using a process developed by them for high-power laser array applications [91]. The next subsection will present an E-o-E compatible VCSEL structure.

IPSEL fabrication begins with a modified in-plane laser diode heterostructure. There are two additional design considerations for IPSELs. First, the active region
Figure 3.38: IPSEL fabrication with IBAE. (a) Laser heterostructure (far left) with vertical mirror (left) and parabolic deflector (right) etch. IPSELs can be fabricated in DGWs by matching the total growth thickness to the dielectric sidewall (far right) height. (b) Geometric model for calculating parabolic mirror etch times to be used in IBAE parametric control software. Figures based on [92].
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depth from the top surface must be matched to the deflecting mirror that will eventually be fabricated. In the present work, the active region depth was set to 2.5 μm to couple into a parabolic mirror. The second consideration is the collection efficiency of the parabolic mirror. The mirror must be positioned in such a way that maximum laser emission is collected and redirected upward. For typical parabolic mirror dimensions and placement, which will be described shortly, an output beam divergence of ~35° and parabolic deflector f-number of ≤0.85 results in ~87% collection efficiency [93]. A larger beam divergence would require the deflector to be brought unrealistically close to the laser emission facet. These considerations are illustrated in Figure 3.38 (a). In this figure, only the right most part of the laser is shown and a dielectric sidewall is pictured, which suggests how an IPSEL can be fabricated in a DGW (detailed in Subsection 4.6.2). The active region depth can be controlled during epitaxial growth, typically requiring a spacer layer on top of the diode structure, and the beam divergence can be decreased by widening the transverse optic mode of the laser cavity.

After the heterostructure is grown, vertical cavity mirrors and the parabolic mirror must be etched. Argon ion-beam-assisted etching (IBAE), in a background of chlorine, is a dry-etching technique which produces extremely smooth sidewalls ideal for laser mirrors [94, 95, 96]. The first step is to etch the vertical laser facets. A 4× e-beam generated optical mask and a 4:1 projection aligner were used to pattern a 1.0-μm-wide line at one end of the laser cavity and a 10.0 μm line at the other end. With the photoresist as an etch mask, perpendicular IBAE was used to etch straight-sided ~4.0-μm-deep grooves. The 4× mask and projection reduction improves the smoothness of the photoresist edge and, thereby, improves the smoothness and quality of the facets. A detailed IPSEL process flow is presented in Appendix B. The photoresist is then stripped leaving longitudinally defined laser cavities. A scanning electron micrograph (SEM) of this etch, termed IBAE1, is shown in Figure 3.39.

The next step is to etch the parabolic deflecting mirror at one end of each IPSEL.
Figure 3.39: 45° SEM top-view of vertical laser mirror facet (IBAE1).

Figure 3.40: 30° SEM side view of parabolic mirror sidewall (IBAE2).
Parabolic mirrors could be fabricated next to both mirror facets, to redirect all emission from the laser. This requires two separate etches and was not included in this work. A 3.5-µm-wide line was opened in a new layer of photoresist, with a 1× e-beam-written contact mask, immediately adjacent to the outside edge of the facet groove. See Figure 3.38 (a). The parabolic deflector was then formed by parametrically rotating the sample while etching (computer-controlled angled IBAE). In this technique, the angle of the sample with respect to the ion beam is stepped during the etch to achieve the desired parabolic curvature. Figure 3.38 (b) illustrates the relation between the desired curve to be etched and the line segments programmed into the IBAE system. The step-wise approximation to a parabola consists of n line segments, where n is typically several hundred. The time that the sample is maintained at a particular angle (φn) with respect to the ion-beam is given by

\[ t_n = \frac{L_n}{r \cos(\phi_n)} \]  

(3.30)
where $L_n$ is the step length in the $\phi_n$ direction (see Figure 3.38 (b)) and $r$ is the etch rate. A 3.5 $\mu$m-deep-parabola typically takes 45 minutes with a typical etch rate of etch rate 200 $\AA$/min. An SEM of this etch, termed IBAE2, is shown in Figure 3.40. An SEM of IBAE1 and IBAE2, with the IBAE2 photoresist left on demonstrating the photoresist protection of the laser mirror facet (IBAE1 groove), is shown in Figure 3.41. The laser facet can faintly be seen buried under the protecting photoresist (middle right of SEM).

The final etch step forms the 2.1-$\mu$m-deep ridge waveguide. The etch depth is designed to produce a single lateral optic mode and is quite deep because of the top spacer layer used to position the active region 2.5 $\mu$m below the surface. A 1 $\times$ e-beam-written contact mask was used to pattern a 4-$\mu$m-wide photoresist line extending 360 $\mu$m, from facet to facet. Vertical IBAE, identical to IBAE1, was used to etch the ridge as seen in SEM shown in Figure 3.42.

Figure 3.43 is an SEM of all three IBAE etches (IBAE1, 2 and 3). The ridge waveg-
Figure 3.43: 45° SEM top view of all three IPSEL IBAE etches (IBAE1, 2 and 3). The ridge waveguide is seen on the right and the parabolic deflector is seen on the left. The top-surface morphology is due to unusually high p-type (Be) top-contact layer doping and not IPSEL processing.
uide is seen on the right and the parabolic deflector is seen on the left. The “T” at the end of the waveguide was fabricated to avoid damaging the mirror facet during ridge waveguide formation (IBAE3). The top surface appears rough because the p-type Be doping concentration was too high during the laser growth. Consequently, this roughness partially translated into sidewall roughness due to non-uniform photoresist.

The final two IPSEL fabrication steps are electrically insulating dielectric deposition and metallization. A half-wavelength of SiO₂, as measured on the vertical facet sidewalls, was PECVD deposited over the entire structure. This layer serves two functions. First, this layer isolates subsequent ohmic metal from the laser structure everywhere except in areas where vias are wet etched. Second, the half-wavelength of dielectric coats the laser end facets but does not form parasitic high-reflection (HR) or antireflection (AR) layers. After vias are opened in the SiO₂ to accommodate p-type ohmic contacts, Ti/Au was angle evaporated twice. Angle evaporation is necessary to coat both the parabolic mirror and the opposite end mirror facet. Coating the parabolic deflector increases its reflectivity and coating the opposite mirror facet forms an HR layer. In addition to this angle, a rotation in an orthogonal direction is necessary to coat two of the sidewalls formed during the ridge waveguide etch (IBAE3). Two angled evaporations, each these two rotations, are needed to coat all four sidewalls, thereby achieving good step coverage for the p-type ohmic contact metal lines. These evaporations are lifted off to complete IPSEL fabrication.

Figure 3.44 is a 50× top view optical photograph of completed IPSELS (8 shown on left), LED structures (9 shown on right) and process alignment marks (lower-middle right). Figure 3.45 is a 200× top view optical photograph of completed IPSEL. Figure 3.46 is a 400× top view optical photograph of completed IPSEL. Parabolic mirror and associated laser facet are on the left. Unfortunately, the final angled Ti/Au evaporation was fired in the wrong orientation and both end facets were Ti/Au coated. Time did not permit another fabrication sequence.

For optimized laser heterostructures, typical IPSEL operating characteristics in-
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Figure 3.44: 50× top view optical photograph of completed IPSELs (8 shown on left), LED structures (9 shown on right) and process alignment marks (lower-middle right).

Figure 3.45: 200× top view optical photograph of completed IPSEL.
Figure 3.46: 400× top view optical photograph of completed IPSEL. Parabolic mirror and associated laser facet are on the left.

clude threshold currents \( \sim 200 \, \text{A/cm}^2 \), \( \eta_d \sim 65\% \) and cw operation [97]. These values are nearly identical to the characteristics measured from cleaved-facet devices fabricated in the IPSEL material. In addition, the parabolic mirror can reduce the far-field transverse divergence angle from \( \sim 35^\circ \) FWHM to about \( 13^\circ \) FWHM, as expected for a 3.5-\( \mu \)m-wide aperture, which is important for both free space optical interconnection and efficient optical fiber coupling applications. IPSELS with less complicated mirror formation processes (e.g. RiE angled sidewall deflectors) and fabricated in different material systems (e.g. (In,Ga)AsP) are also possible and are also compatible with the E-o-E integration technique.

3.3.4 Vertical-Cavity Surface-Emitting Lasers

Vertical-cavity surface-emitting lasers (VCSELS) are attractive optical emitters for optoelectronic integrated circuits for several reasons. These attributes include extremely small lateral dimensions (footprint), typically 10 \( \mu \)m × 10 \( \mu \)m, and a low-
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divergence circular output beam which is advantageous for free-space interconnects and efficient single-mode fiber coupling. Historically, however, there have also been several drawbacks to the VCSEL structure, though rapid progress in the past five years has significantly reduced most of these shortcomings.

First, VCSEL structures require two very high reflectivity (>99%) DBR mirrors on either side of the active gain region. DBR mirrors are typically formed during epitaxial growth by stacking quarter-wavelength-thick layers of material with alternating refractive indices. (Al,Ga)As based DBR pairs often consist of GaAs and AlAs with a relatively small difference in index of refraction between these layers (3.5-3.0). Because of this small index difference, the stop band is narrow (∼ 100 nm) and a large number of pairs must be stacked to achieve the necessary reflectivity (>20). To assure that the cavity resonance is aligned with the gain peak, the layer thicknesses must be controlled to within ±1%. Such precise growths were historically difficult to control, but they are now routine particularly with recently developed in situ thickness measurement techniques [98, 99]. A straightforward way to reduce the demands on layer control is to use DBR pairs with larger index differences. Dielectric mirrors such as SiO₂-SiNₓ or Sb₂S₃-MgF₂ have significantly larger index differences which result in a wide stop band and high reflectivity with just a few pairs. Though these DBRs are deposited after epitaxial growth of at least the active region, and can therefore take advantage of tuning the DBR center frequency to match the gain peak, it is difficult to fabricate VCSELs with dielectric mirrors on both sides of the active region. Even a single dielectric mirror, on the top surface for example, can reduce the total stack thickness, however. A recent solution to the need for a high index difference DBR pair, which can be formed as easily as epitaxial layers, is the use of oxidized AlAs. AlAs can be oxidized by wet oxidation of AlGaAs, at ∼ 425°C for ∼ 10 min, without significantly affecting surrounding GaAs layers [100, 101, 102]. The resulting AlAs oxide index of refraction is 1.55 and the thickness is 90% of the original AlAs [103]. DBR stacks with as few as four pairs of quarter-wavelength AlAs oxide-GaAs layers
Figure 3.47: VCSEL structure compatible with E-o-E integration. A four pair AlAs oxide-GaAs top DBR and an AlAs oxide current constriction layer have been used to achieve threshold currents as low as 0.22 mA for apertures as small as an 8 μm square [105].

have achieved \(>99\%\) reflectivity with a stop band width of \(\sim 600\) nm. Photopumped [104] and, most recently, electrically pumped VCSELs using AlAs oxide DBRs have been reported [105]. Such a device is illustrated in Figure 3.47.

A second concern about using VCSELs in optoelectronic circuits has been high threshold voltages. Until roughly three years ago threshold voltages were typically \(>5\) V due to high-resistance DBR mirrors which, in addition to forming the optical cavity mirrors, conduct the laser pump current. Grading the large conduction and valence band discontinuities reduced this voltage drop, but eventually contact schemes were used to completely avoid the p-type mirror. Threshold voltages are now typically \(\sim 2.0\) V which are compatible with optoelectronic circuits, including the voltage han-
dling capabilities of the GaAs MESFET circuitry used in the E-o-E technique. See Figure 3.47.

A final VCSEL issue has been current confinement which governs the threshold current. Two approaches to current confinement have been high resistivity proton-bombardment and mesa etching. Both of these techniques channel the terminal current through a narrow lateral area in an attempt to reduce the total threshold current (total threshold current = threshold current density × area). Threshold current scale-down has been limited by the increasing threshold current densities associated with decreasing areas, especially in the case of etched mesas, because of surface recombination. Passivation techniques, such as sulfur passivation, have helped but the real innovation has come, once again, from oxidized AlAs [105]. An AlAs layer can be wet oxidized from the perimeter of a large etched mesa. By controlling the radially inward progression of this electrically insulating AlAs oxide (e.g. timing the reaction with a known oxidation rate) an extremely small current confining aperture can be formed. This aperture determines the lateral area of the gain region that is electrically pumped and, therefore, determines the overall threshold current. A VCSEL employing this AlAs oxide aperture technique has recently been reported [105] (see Figure 3.47).

These VCSEL advances have been incorporated into a single structure by Dapkus and coworkers [105], which is schematically illustrated in Figure 3.47. The key features are the four pair AlAs oxide-GaAs top DBR and the AlAs oxide current constricting layer. Threshold currents as low as 0.22 mA for apertures as small as an 8 μm square have been achieved. Threshold voltages are a bit high (~2.5 V) should be able to be reduced by either grading the lower DBR layers or including an n-type contact above this DBR stack. Even in present form, these drive characteristics are compatible with E-o-E MESFET circuits. The wet oxidation is performed at a temperature which is also compatible with the E-o-E integration technique (~ 425°C for ~ 10 min) and the total thickness can be slightly adjusted to match the dielectric sidewall height. A remaining question is if the layers can be grown at temperatures compatible with
Figure 3.48: Reflection spectra from three 16 period AlAs/Al$_{0.11}$Ga$_{0.89}$As DBRs grown at 600°C, 500°C and 400°C [77]. The variation in center frequency is due to layer thickness calibration variances, not temperature effects.

The E-o-E integration technique (i.e. ≤470°C). The structure reported [105] was grown by MOCVD which has a growth temperature typically well above 600°C. This structure can also be grown by either conventional MBE or by lowered-temperature MBE techniques. It is probable that the AlAs oxidation reaction will not be affected by reduced growth temperature AlAs. To confirm that the optical reflection properties of DBRs are not significantly affected by reducing the growth temperature to as low at 400°C, three DBRs were grown at various temperatures. Figure 3.48 shows the reflection spectra from three 16-period AlAs/Al$_{0.11}$Ga$_{0.89}$As DBRs grown at 600°C, 500°C and 400°C by conventional MBE with a reduced As overpressure. The variation in center frequency is due to layer thickness calibration variances, not temperature effects. This demonstrates that DBR peak reflection and stop band width are not affected by reducing the growth temperature to as low at 400°C. As will be shown in Subsection 3.4.2, the voltage drop across this DBR is also acceptable.
3.4. OPTICAL MODULATORS

VCSELs are now well positioned to be integrated with electronic circuitry. The E-o-E optoelectronic integration technique can readily accommodate VCS L structures and, with four levels of interconnect metal in the Vitesse process, extremely large smart pixel VCSEL arrays should be possible.

3.4 Optical Modulators

Optical modulators are devices which convert electrical signals into optical signals by varying the phase or amplitude of continuous wave optical signal. For certain applications, such as high-frequency modulation, extremely high density arrays, low electrical power arrays and coherent optical processing, optical modulators are preferable to optical emitters [112, 113]. Optical modulators can be either in-plane or surface-normal, depending on the propagation direction of the modulated light with respect to the plane of the optoelectronic chip. Subsection 3.4.1 will briefly review an in-plane modulator structure designed and fabricated by fellow members of the NCIP1 consortium [125] established to advance the E-o-E integration technique. Subsection 3.4.2 is overview preliminary work on surface-normal MQW modulators for use in S-SEED and FET-SEED optoelectronic circuits. The E-o-E optoelectronic integration technique includes enhancement-mode MESFETs, in addition to depletion-mode MESFETs, which should allow E-o-E FET-SEED circuits to operate at a lower power and be designed with greater flexibility than the AT&T FET-SEED process [108].

3.4.1 Hetero-nipi — In-Plane Modulators

In-plane waveguides and modulators are essential components for photonic integrated circuits (PICs), which is a class of optical circuit which traditionally has few discrete electronic components. By designing narrow, and possibly long, dielectric growth wells it is possible to use the E-o-E technique to integrate semiconductor waveguides and modulators with VLSI GaAs MESFET circuitry. An impor-
Figure 3.49: Hetero-nipi in-plane phase modulator compatible with the E-o-E integration technique. The "/" lines indicate Si-implanted n-layer contact implant and the "\" lines indicate Be-implanted p-layer contact implant. Figure modified from [109].
3.4. **OPTICAL MODULATORS**

tant consideration for modulators, which are typically phase modulators for use in a
Mach-Zehnder interferometer configuration, is the voltage-length product necessary
to change the optical phase by $\pi$ radians. This product $(V_\pi \times L)$ is typically too high to
achieve a $\pi$ phase shift with MESFET compatible voltages (e.g. $< 5$ V) in distances
reasonable for integration with VLSI electronics (e.g. $< 1$ mm). To address these
issues, Steffen Koehler [106] (Garmire's group at USC and member of the NCIPT
consortium to advance the E-o-E technique) and members of Fonstad's group at MIT
[107] set $(V_\pi \times L)$ target of $2$ V $\times 300$ $\mu$m. The maximum Al mole fraction ($x$ in
any $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer) was also restricted to $x \leq 0.10$ to be compatible with lowered
temperature, conventional MBE growth. Finally, the total heterostructure thickness
should be $\leq 4.2$ $\mu$m to match the top surface of the dielectric growth well sidewall and
all processing steps should be low temperature. This was an extremely aggressive set
of specifications which Koehler and Garmire essentially achieved [109].

A n-i-p-i heterostructure [110, 111], so called because of the multiple n, i and p
layers, was selected because of its increased interaction with the optic mode, in a
single-mode modulator, and therefore promised the lowest $V_\pi \times L$. The electric field
and optical confinement were optimized in order to maximize the phase change for
a given applied field and device length. The design variables included the thickness
of the doped regions, the doping concentrations, the number of intrinsic regions, the
compositions of any cladding layers and the thickness of the intrinsic regions. An
algorithm was developed as part of Koehler's work to facilitate future optimizations
for different specifications. The final heterostructure is shown in Figure 3.49.

The heterostructure was MBE grown at 690°C. While this is outside the con-
straints set by the E-o-E technique, the heterostructure layers should perform well at
growth temperatures below 500°C as gauged by the performance of other devices.
Standard photolithography and wet etch techniques were used to form the ridge
waveguide. A photoresist-patterned, angled (30°) Si-implant was then performed to
achieve a concentration of $2 \times 10^{18}$ cm$^{-3}$, to a depth of 4000 Å, in the ridge waveguide
sidewall. This was followed by 3000 ÅAu/Sn (n-type contact) e-beam evaporation followed by an ultrasonic-assisted liftoff. A similar angled Be ion-implantation was performed followed by Au/Zn metallization to achieve contact to the p-type layers. The final step was a 500°C anneal for 30 sec to activate the implants and to alloy the contact metal.

Koehler characterized the optical modulators (λ = 990 nm) and a π phase change was achieved with a 0.62 V applied bias and a 1.24-mm-long device. This corresponds to a V × L of 0.77 V-mm which scales to a π phase change at 3.1 V for a device length of 300 μm. The 1.24-mm-device has a critical frequency at 110 MHz while the scaled down device should have a critical frequency near 200 MHz [109]. These results indicate that phase modulators that are voltage, geometry and process compatible with the E-o-E integration technique are possible.

### 3.4.2 MQWs/SEEDs — Surface-Normal Modulators

MQW modulators/detectors and SEED circuits [114, 115] have been pioneered over the past decade by Millen and coworkers at AT&T Bell Labs [116]. The success of these optoelectronic circuits derives from the quantum confined Stark effect (QCSE) [78] which explains how excitonic absorption peaks can be shifted by several times their zero-field binding energies. Room-temperature, high-contrast-ratio modulators are therefore possible. Numerous bistable SEED circuits have been demonstrated over the past decade. These circuits clarified the need for electronic gain stages (i.e. transistors) to be monolithically integrated with the optical MQW modulators, which also serve as detectors, in order to keep optical switching energies \( \hbar \omega \) (e.g. \( \sim 100 \, \text{fJ} \)) [117]. This led the AT&T groups to develop a D-MESFET - MQW modulator/detector monolithic integration process termed the FET-SEED process [118, 108, 119]. FET-SEED circuits are comprised of MQW detectors which feed into D-MESFET receiver circuits, a variety of D-MESFET based electronic logic and D-MESFET based output stages which control the voltage across output MQW modulators. The same MQW
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Figure 3.50: GaAs/AlGaAs MQW modulator/detector heterostructure compatible with the E-o-E optoelectronic integration technique [72].

The heterostructure serves as both detector and modulator. There are two drawbacks to the FET-SEED process. First, all electronic circuits are fabricated in epitaxial layers grown on top of the MQW modulator. As reviewed in Chapter 1, this is a reasonable approach except that backgate shields must be grown and contacted to isolate the FETs from the MQW layers. A related issue is that FET threshold control is also difficult to achieve over large areas, such as a 4-inch wafer. An advantage to growing heterostructure-based MESFETs is that the breakdown voltage can be high (e.g. ~10 V) which is advantageous for driving large voltages across MQW modulators, thus achieving a high modulator contrast ratio. The second drawback to the FET-SEED process is that only DFETs are offered. This restricts design flexibility, requires additional voltage rails and consumes greater power than an E/D process.

With this overview of the AT&T FET-SEED process, both merits and limitations, it is reasonable to assess the E-o-E optoelectronic integration technique for use with MQW modulators. To evaluate this possibility a heterostructure was de-
Figure 3.51: Photoluminescence spectrum of the MQW layers grown at 500°C.

The process and measured by our collaborator J. Luo at Caltech [72] and the heterostructure was grown by reduced-temperature MBE at MIT [77]. The layer structure was presented in the p-i-n optical detector discussion (Subsection 3.2.4) and is repeated in Figure 3.50 for convenience. This heterostructure consists of a p-type cap layer above an intrinsic MQW absorption region which is, in turn, above an n-type DBR mirror. This structure was designed for 840 nm, at zero applied field, operation. The total number of wells was decreased (e.g. 70 instead of typically 90) to reduce the required applied reverse voltage to achieve a reasonable on/off contrast ration (e.g. 3). Shallower quantum wells and triangular wells can also be used to reduce the required voltage swings [120, 121, 122]. Low-voltage operation is essential for integration with Vitesse MESFETs which have a drain-source breakdown of ~5 V. Circuits can be designed to swing up to ~8.5 V as discussed in Subsection 4.7.8.

Various growths were conducted at MIT [77] to prove the constituent parts of
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Figure 3.52: I-V characteristics of the full SEED heterostructure grown at 500°C.

This total SEED structure. To confirm that the optical reflection properties of DBRs are not significantly affected by reducing the growth temperature to as low as 400°C, three DBRs were grown at various temperatures. Figure 3.48, in the previous subsection, shows the reflection spectra from three 16-period AlAs/Al0.11Ga0.89As DBRs grown at 600°C, 500°C and 400°C by conventional MBE with a reduced As overpressure. The variation in center frequency is due to layer thickness calibration variances, not temperature effects. This demonstrates that DBR peak reflection and stop band width are not affected by reducing the growth temperature to as low as 400°C. To confirm that the absorption peak is strong at the reduced growth temperature of 500°C, just the MQW layers were grown. Figure 3.51 shows the photoluminescence spectrum of the MQW layers. The MQW absorption peak is strong and is on the left (higher energy) of the GaAs peak. The entire SEED structure was then grown at MIT (500°C growth temperature) and processed and measured at Caltech. Figure 3.52 is the I-V characteristics of the structure showing a strong forward bias turn on indicating that at most a few tenths of a volt are dropped across the lowered-temperature DBR stack. The reverse bias characteristic shows less than 10 nA of current flowing
at -15 V bias which is a typical dark current for this class of heterostructure. The optical responsivity spectrum (photocurrent), at various reverse biases, of the full SEED structure was presented in the p-i-n optical detector discussion (Subsection 3.2.4) and is repeated in Figure 3.53 for convenience. The MQW zero-field electron-heavy hole (ehh) exciton peak is centered at \( \sim 8380 \) Å and can be red-shifted by \( \sim 7 \) nm with an applied reverse bias of -8 V. The ehh exciton absorption peak remains strong out to -8 V with roughly a 10% decrease in responsivity. This indicates that the layer quality is sufficient for the exciton to persist at typical operating fields. Figure 3.54 is the reflection spectrum, at various applied reverse biases, of the full SEED heterostructure grown at 500°C. At the operating wavelength of 840 nm (\( \lambda_0 \) operation), the contrast ratio is nearly 2:1, which is reasonable considering that these devices were not AR coated, reducing the optical intensity reaching the MQW. For a flat, infinitely wide stop band DBR the reflection spectrum (Figure 3.54) should be the inverse of the absorption spectrum (Figure 3.53). The long-wavelength region (841 nm and higher) of the reflection spectrum does not follow this trend. The maximum modulation depth of the -8 V curve, for example, is not as deep as would be expected from the photocurrent spectrum. The photocurrent measurement is not as sensitive to the DBR spectrum as is the reflection measurement. This suggests that the DBR long-wavelength stop band edge is clipping the characteristic at wavelengths longer than \( \sim 841 \) nm. Better control of the DBR center frequency or use of a GaAs-AlAs oxide DBR, to achieve a very wide stop band, should be pursued to correct this feature and to enable \( \lambda_1 \) operation (i.e. \( \lambda \) of absorption peak at maximum applied field).

These preliminary measurements are encouraging and indicate that a FET-SEED technology based on the E-o-E optoelectronic integration should be possible. To further explore this idea, several basic FET-SEED circuits were designed and fabricated on the MIT-OEIC-3 chip [58] (see Subsection 4.7.7).
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![Graph](image)

Figure 3.53: Photocurrent spectrum, at various reverse biases, of the full SEED heterostructure grown at 500°C.

![Graph](image)

Figure 3.54: Reflection spectrum, at various reverse biases, of the full SEED heterostructure grown at 500°C.
Chapter 4

E-o-E OEIC Demonstrations

The previous chapter presented several optical and electrical devices which are compatible with the E-o-E optoelectronic integration technique. These devices can, therefore, be used in numerous combinations to build functional E-o-E based OEICs. This chapter presents several functional and diagnostic demonstration OEIC chips. The functional OEICs perform particular optoelectronic signal processing functions while the diagnostic OEICs provide design and process information used for subsequent OEICs.

Five neural-inspired OEIC chips were designed and fabricated in collaboration with A.C. Grot and D. Psaltis at Caltech [69, 123]. Each chip built on previous designs and tested new circuit and process ideas. These chips are termed Generation 1-5 (Gen. 1-5) to reflect their evolutionary relationship and are detailed in Subsections 4.1-4.5. Gen. 1 demonstrated an optoelectronic threshold circuit, with OPFET detectors and LED emitters, and was fabricated by growing LEDs on two-thirds of a chip. Gen. 2 and Gen. 3 developed lithographically defined foundry-etched DGWs with S/D ion-implantations and ohmic contacts. A 3-unit winner-take-all (WTA) optoelectronic circuit was demonstrated, and fully simulated, with the Gen. 4 chip, and the Gen. 5 chip included a 100-unit two-dimensional WTA circuit array.

High-speed transmit and receive OEICs were explored with the MIT-OEIC-1,2
CHAPTER 4. E-O-E OEIC DEMONSTRATIONS

chips. The electronic circuits on these chips were designed by P.R. Nuytkens at MIT [75, 124]. MSM detectors with transimpedance amplifiers and laser drivers were designed and tested. LEDs, in-plane lasers and IPSELs were separately integrated on these chips. Electronic circuit testing is described in Section 4.6 and LED and IPSEL integration is discussed in Subsections 4.6.1 and 4.6.2, respectively.

To explore the variety of optical and electrical devices that can be integrated with VLSI GaAs MESFET circuits via the E-o-E technique, a multi-epitaxy chip termed MIT-OEIC-3/NCIPT-OEIC-1 was designed and fabricated [58, 125]. The multi-epitaxy concept is that a single chip can have subregions with circuits specific to a particular optical device. Because a MOSIS/Vitesse fabrication run typically returns \(~100\) chips, though only \(~25\) are quoted, there is a sufficient number of chips to dedicate an entire chip to a given epitaxial sequence even though this results in mismatched circuit-optical devices in certain areas. This is an effective way to explore a large number of circuit-epitaxial device pairings. This multi-epitaxy chip includes circuit designs from most NCIPT member groups. The following optoelectronic circuit categories are present on this chip: process, detector, LED, laser, transceiver, RTD-based SRAM, SEED, in-plane modulator and thermal stability. Section 4.7 further describes this chip.

The final OEICs discussed in this chapter are on a chip that explores compact “optical bond pads,” termed MIT-OEIC-4 [126]. “Optical bond pads” (OBPs) are optical input and output devices with associated electrical drive and receive circuitry. These OBPs are functional optical interconnects with performance benefits previously discussed in Chapter 1. A portable collection of OBP “drop-in” cells can be included in a standard optoelectronic cell library, which is resident within a commercial circuit CAD package. OBPs are intended to replace electrical signal bond pads. Section 4.8 overviews this OBP chip.
4.1 Neural Thresholding Circuit Chip (Gen. 1)

Highly parallel neural networks is one class of computing architecture that can benefit from large-scale high-density two-dimensional OEIC arrays. Each neuron in an array must receive signals from surrounding neurons, compute a nonlinear function based on these inputs and transmit signals both to surrounding neurons and back to itself. In the human brain, which suggests an ultimate size and density scale for neural circuits, there are approximately $10^{11}$ neurons (somas) and each neuron has on average roughly $10^3$ connections (synapses) [127]. This extremely large number of connections from each neuron to surrounding neurons and to itself limits the success of all-electrical implementations and has led researchers to pursue optoelectronic implementations [128]. Electrical circuits must use electrical interconnect lines, which are in the plane of the chip, to interconnect all neurons in an array. The area required for the electrical interconnects limits the number of neurons on a chip to a few hundred [129]. OEICs, however, can use optical interconnects, which are often free space and surface-normal, while still performing nonlinear functions with electronic devices. This is the benefit of optoelectronic circuit based neural networks.

Perhaps the most fundamental neural computation is the threshold function. Each neuron must sum the product of its inputs ($X_i$) and the associated interconnection weights ($w_{ij}$) and then compare this summation to a threshold value. If the sum is larger than the threshold value then the neuron output ($Y_j$) should be on, otherwise the neuron output should be off. The transition from off (low) to on (high) does not need to be extremely sharp and is often expressed using the hyperbolic tangent function

$$Y_j = A \tanh \left( \sum_{i=1}^{N} w_{ij} X_i \right)$$

(4.1)

where $A$ is the gain and $N$ is the number of input neurons. An optoelectronic threshold circuit can be used in neural circuits to approximate the $tanh$ function necessary to calculate the output. The calculation can be done using analog electronics while
both the input and output signals are optical. Another need for an OE threshold circuit is to calculate $w_{ij}$ during the network training phase. The back error propagation (BEP) algorithm, for example, changes $w_{ij}$ by an amount proportional to the error between the actual output and the desired output. Both the actual output (i.e. $Y_j$) and the desired output are optical signals and the required error signal can be computed with simple electronic circuitry and an OE threshold circuit [70].

While an optoelectronic threshold circuit is useful in numerous other applications (e.g. non-neural), the previous discussion shows the importance of this simple circuit for a developing computation architecture. With neural network applications in mind, optoelectronic threshold circuits, for both input and output thresholding, were designed and fabricated in collaboration with A.C. Grot [69, 123] and D. Psaltis at Caltech [71, 130, 131, 132].

E-o-E based input thresholding circuits can be built in a variety of ways which use one or more OPFETs as the optical detector(s) and either an EFET, a DFET or another OPFET as the threshold control element. The optical input(s) (i.e. $X_i$) impinge on the OPFET(s) which are connected in parallel with one terminal connected to a DCFL rail. The threshold value is either a voltage, in case of the EFET or DFET, or another optical signal, in the case of an OPFET. In all cases the threshold control element is connected between the other DCFL rail and the other OPFET(s) terminal. This configuration is very similar to a multiple-input DCFL NOR circuit where the input EFETs have been replaced by OPFETs and the pull-up DFET has been replaced by and EFET, DFET or OPFET. These circuits do not require an epitaxial growth step and have been successfully demonstrated [70].

An E-o-E based output threshold circuit can be fabricated by connecting an optical emitter in series with a DFET. The electrical input to this circuit is the voltage across the series pair, the threshold value is the gate bias on the DFET and the optical output is the LED optical output power. While other threshold circuits are certainly possible, this simple circuit, named Generation 1 (Gen. 1), served as the initial demonstration
4.1. NEURAL THRESHOLDING CIRCUIT CHIP (GEN. 1)

of the E-o-E optoelectronic integration technique. Gen. 1-5 chips were designed by A.C. Grot at Caltech [69] in communication with MIT [123].

The LED for the OE threshold circuit requires an epitaxial growth step. For this initial demonstration, the growth region (precursor to DGW) was specified by designing a single, large (2 mm × 3 mm) blank area on the chip (3 mm × 3 mm). This area did not contain electronic circuitry, was not ion-implanted and did not have the dielectric layers removed at Vitesse. DFETs (13.6 μm × 2.8 μm), several test circuits and OPFET detectors were designed and placed in the remaining area (1 mm × 3 mm) of the chip.

After the chip was fabricated at Vitesse (HGaAs2 technology through MOSIS), the circuit area of the chip (i.e. 1 mm × 3 mm region) was protected with black wax and the dielectric layer stack was removed with a wet chemical etch (HF:DI H2O 1:10 for approximately 10 min.). This exposed the underlying semi-insulating (actually slightly p-type) GaAs crystal in the growth region while preserving the electronic circuits. The black wax was removed with acetone and the chip was degreased. An O2 plasma strip was then performed to thoroughly remove the wax residue. In preparation for MBE growth, the chip was once again degreased and dipped in buffered-oxide etchant to minimize the native oxide thickness.

The chip was indium solder mounted on a molybdenum block at the perimeter of a quarter of a 2-inch-diameter GaAs wafer (semi-insulating, epitaxy-ready wafer from AXT Corp.) which served as a control wafer as well as a pyrometer source and a RHEED crystal. The block, with mounted samples, was ramped up to 580°C at 15°/min. After the native oxide desorbed from the control wafer (~1 min at 580°C) and an additional 5 minutes at 580°C, the native oxide on the growth region of the chip was assumed desorbed. The As flux was turned on only after the native oxide desorbed in an attempt to speed desorption and increase desorption uniformity. A not-intentionally-doped (N.I.D.) GaAs/AlGaAs superlattice was initiated at 580°C after which the block temperature was ramped to 530° at 15°/min. The superlattice
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<td>1 × 10¹⁶ p</td>
</tr>
<tr>
<td>Al₀.₃Ga₀.₇As</td>
<td>3000</td>
<td>6 × 10¹⁷ p</td>
<td>3000</td>
<td>1 × 10¹⁸ p</td>
</tr>
<tr>
<td>GaAs</td>
<td>5000</td>
<td>5 × 10¹⁸ p</td>
<td>5000</td>
<td>5 × 10¹⁸ p</td>
</tr>
<tr>
<td>GaAs/Al₀.₃Ga₀.₇As</td>
<td>5000</td>
<td>N.I.D.</td>
<td>5000</td>
<td>N.I.D.</td>
</tr>
<tr>
<td>(superlattice)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Substrate</td>
<td>625 µm</td>
<td>S.I.</td>
<td>625 µm</td>
<td>S.I.</td>
</tr>
</tbody>
</table>

Table 4.1: LED heterostructures grown on Gen. 1 chips.

was grown to impede upward propagation of defects from the semi-insulating substrate. A p-side down LED heterostructure was grown with a total growth time of nearly 4 hours at the lowered growth temperature of 530°C. Table 4.1 shows two LED heterostructures grown on two different Gen. 1 chips (no performance difference was observed). A lowered arsenic overpressure (e.g. III/V ratio of approximately 3) was used during the growth and the 530°C growth temperature was selected because of its minimal effect on the ohmic contacts and intrinsic FETs. Interlevel metal degradation at this temperature was not quantified at the time of this experiment. After the LED growth was complete the block was ramped down to room temperature at 15°/min and the samples were dismounted from the block. The back-side indium was removed by protecting the top side of the chip with black wax and etching the indium with 1:1 HCl:DI H₂O at ~90°C for roughly 15 min. This completed the LED growth sequence.

To complete the OE threshold circuit, LEDs were fabricated in the epitaxial layers. First the polycrystalline material that covered the circuits on the chip was selectively removed by masking off the epitaxial region with photoresist and then wet etching the poly-material. The chip was dipped in room temperature phosphoric-based etchant (H₃PO₄:H₂O₂:H₂O 1:1:5) until the dull gray poly-material color, which covered the dielectric stack, was observed to change to the bright green color of the dielectric
stack, indicating that the poly-material was completely removed. This took about 3 min and a 30 sec overetch was included to further clean the aluminum pad areas (phosphoric acid does not significantly etch Al in 30 sec). After the photoresist was stripped the chip was sent to Caltech for LED processing.

Because the chips are small (3 mm × 3 mm), the chip and scrap material of identical thickness (spare Gen. 1 chips) abutted to the edge of the grown chip were mounted with soft-baked photoresist to a carrier silicon wafer. This reduced the photoresist buildup at the edge of the chip by effectively extending the height step to the edge of the scrap material (this led to the idea of a custom spin-chuck). This technique was used for all photolithography steps.

The epitaxial layers were wet etched (phosphoric acid:hydrogen peroxide:acetic acid 1:1:6) down to the bottom p-GaAs layer to form LED mesas (130 μm × 170 μm). 1000 Å of CVD Si₃N₄ (610°C for 5 min) was deposited to electrically insulate the contact metal from the heterostructure. Contact vias were then etched through the Si₃N₄ to the n-GaAs and p-GaAs contact layers for subsequent n- and p-type ohmic contact metallization. N-type and p-type ohmic contacts, AuGe/Ni/Au (300 Å/100 Å/1000 Å) and AuZn/Au (300 Å/1000 Å) respectively, were then evaporated and lifted off. Finally, the metal was alloyed (410°C for 2 min), thereby completing the LED process flow.

An optical photograph of the completed Gen. 1 optoelectronic chip is shown in Figure 4.1. The MESFET circuits are on the right and the LEDs in the epitaxial growth area are on the left. The boundary between the circuits/dielectric stack and the LED/growth area is in the middle. The boundary is curved due to the crude hand-painted black wax dielectric etch mask and the dark border along the boundary is due to wet etch undercut. The cracks visible over the circuits are in the top dielectric, overglass, layer and do not appear to interfere with the operation of the circuits underneath. The cracking can be reducing by lowering the maximum growth temperature and substrate temperature ramp rate (see Section 5.1).
Figure 4.1: Optical photograph (~ 100×) of the completed Gen. 1 chip showing the MESFET circuits (right) and the LEDs in the epitaxial growth area (left). The boundary between the circuits/dielectric stack and the LED/growth area is in the middle. The boundary is curved due to the crude hand-painted black wax dielectric etch mask and the dark border along the boundary is due to wet etch undercut. The cracks visible over the circuits are in the top dielectric, overglass, layer and do not appear to interfere with the operation of the circuits underneath. The cracking can be reducing by lowering the maximum growth temperature and substrate temperature ramp rate [71].
4.1. NEURAL THRESHOLDING CIRCUIT CHIP (GEN. 1)

Figure 4.2: I-V characteristics of a DFET (L=2.8μm, W=13.6μm and V_{GS} = 0 V) both before and after MBE LED growth [71].

In order to determine the degradation in the MESFET circuits due to exposure to high temperature for a prolonged period, the circuits were electrically tested after the growth and their performance was compared to the original circuit. Figure 4.2 shows the before and after I-V curves for a depletion MESFET with its gate connected to the source. The saturation voltage is the same, whereas the saturation current has decreased by approximately 10%. The source-drain resistance also increased by 40%. The changes are consistent with the thermal cycle data presented in Section 2.1.

In order to estimate the quality of the epitaxial material grown on the chip, the photoluminescence of the epitaxial material was measured and compared with the photoluminescence of the GaAs control wafer which was grown at the same time. An argon-ion laser was used to pump the material and the emitted light was passed through a 0.25 m grating spectrometer with the entrance and exit slits opened to 2 mm. As shown in Figure 4.3, the two photoluminescence peak strengths are comparable indicating that there is not a significant difference in nonradiative recombination
center densities. Because the measurement was conducted at room temperature with wide spectrometer slits, the linewidths should not be used as a figure of merit. Low temperature photoluminescence comparisons with quantum wells will be presented in Section 4.6. The LED material morphology on the chip and on the control wafer looked nearly identical.

The LED efficiencies obtained were low (0.01% at 100 $\mu$A and 0.03% at 1 mA) and had I-V and L-I curves identical to those presented in Figures 3.35 and 3.36 in Section 3.1. This low efficiency is presumably due to the lack of current confinement and the efficiency is approximately the same on the control wafer. Similar LEDs grown at 700°C and identically processed had nearly identical I-V curves and equally low efficiencies, supporting the idea that the low efficiencies were inherent in the structure and are not due to the integration technique.

Finally, LED-DFET optoelectronic threshold circuit was tested. The connection between the LED and the DFET was made by microprobing both the on-chip LED
Figure 4.4: I-V (left vertical axis) and L-V (right vertical axis) curve of grown LED in series with DFET load (see inset circuit). Modified from [71].
and DFET and connecting these terminals externally (future chips monolithically interconnect optical and electrical devices). Figure 4.4 shows the I-V characteristics of the LED in series with the DFET (resistor connected, see inset circuit) on the left vertical axis and the calculated optical output power (Pout) on the right vertical axis (Pout \( \approx I \times 0.0002 \) W/A). This is the desired optoelectronic threshold function. For voltages below 1.0 V Pout is zero. For voltages between 1.0 V and 2.0 V, Pout rises. For voltages between 2.0 V and 5.0 V Pout is saturated at \( \sim 90 \) nW. This operation is simply the result of the \( \sim 1.0 \) V LED threshold voltage, which determines the characteristic below \( \sim 1.0 \) V, and the \( \sim 1.0 \) V \( V_{DS} \) DFET current saturation voltage, which clamps \( I_{DS} \) at \( \sim 0.45 \) mA. The threshold voltage of this threshold circuit is \( \sim 1.5 \) V (voltage at the middle of the transition) and can be increased by placing additional series connected DFETs. The saturation current, and therefore saturation Pout, can be adjusted by sizing the DFET as well as independently controlling the DFET gate.

### 4.2 Dielectric Growth Well Chip (Gen. 2)

The Gen. 1 chip presented in the previous section successfully demonstrated the integration of an LED with a DFET, though roughly two-thirds of the chip area was consumed to integrate just a few LEDs. A more more sophisticated technique to produce dielectric growth wells was needed and the Gen. 2 chip (Vitesse HGaAs2) tested a new approach. As detailed in Subsection 2.2.2, the standard Vitesse passivation and scribe lane RIE etch masks can be stacked resulting in DGWs direct from the circuit foundry. Figure 4.5 is an optical photograph of the Gen. 2 chip, measuring roughly 2.4 mm \( \times \) 2.4 mm, after pre-growth clean as detailed in Subsection 2.4. Circuits with square bond pads (largest bond pads measure 100 \( \mu \)m \( \times \) 100 \( \mu \)m) are around the perimeter of the chip and a single, large (1 mm \( \times \) 1 mm) DGW is in the center of the chip. The DGW appears brighter than the rest of the chip because the exposed GaAs
4.2. DIELECTRIC GROWTH WELL CHIP (GEN. 2)  

crystal at the bottom of the DGW reflects more light that the interlevel dielectric stack. LED heterostructures were grown on Gen. 2 chips, following the procedure presented in the previous section, and the top surface had good surface morphology. LED devices were not processed on these chips because Gen. 3 chips, which were grown at the same time, did have LED devices processed.

The polycrystalline material, which was deposited on the interlevel dielectric stack (i.e. inter-DGW regions) during growth, was removed with a wet chemical etch as described in Section 4.1. The single crystal material was protected from this etch by patterning photoresist (AZ 4620) with a mask which is larger than the DGW by 5 μm in each direction (i.e. 5 μm overhang). It was determined that a 5 μm overhang is an optimal width because the polycrystalline material is roughly 4.5 μm thick, for a 4.2 μm thick single crystalline growth, and polycrystalline material etches isotropically. Therefore, a 5 μm overhang protects the single crystal material during the time it takes to etch the polycrystalline material plus the time for a 15-20% overetch. A wider overhang would leave a polycrystalline bump around the DGW which, unless the overetch time were increased, may affect the bond pad metal. A narrower overhang would allow the poly-strip etchant to reach the edge of the DGW, which could possibly expose the GaAs substrate to the acid. Etching material along the DGW edge and possibly a bit of the GaAs substrate would result in increased step-coverage difficulties due to an enlarged trench. Also, as described in the next section, if the DGW is ion-implanted and the polycrystalline etchant reaches the ion-implanted GaAs substrate the n-type ohmic contact layer would be compromised.

As an aside, two alternate polycrystalline strip techniques should be possible. First, a self-aligned photoresist planarization and RIE etch-back technique was investigated. A thick photoresist (e.g. ~5 μm with SP-20) was applied and spun on an epitaxially grown chip. The wells above the DGWs, with walls formed by the polycrystalline material, were nearly filled with photoresist. The final top-surface was not, however, planar. The photoresist was hard baked and photoresist was ap-
plied and spun again. The top-surface was observed to be nearly planar with a total photoresist thickness of nearly 10 μm. After a final hard bake, photoresist application and spin, the top-surface was planar (≤ ±0.5 μm cross-chip variation). The total photoresist thickness was ~15 μm above the polycrystalline material and ~20 μm above the single-crystal material in the DGWs. O₂ RIE was used to uniformly etch the photoresist back to the top-surface of the polycrystalline material. The single-crystal material in the DGWs retained a nearly 5 μm thick photoresist “cap”. The polycrystalline material was successfully wet-etched. Overetching should be avoided because the wet-etchant may reach the S/D n⁺ ion implant rapidly by following the DGW sidewall, which has uncharacterized epitaxy-dielectric sidewall adhesion properties. The problem with this technique is that the photoresist edge-build is significant (e.g. ~25 μm). This prevented the polycrystalline material around the DGWs within roughly 500μm of the chip edge from being stripped. This technique may prove useful for larger chips, where edge-buildup borders exist. Various photoresist exposure and development combinations were investigated in an attempt to reduce the edge-buildup. Though the edge-buildup was reduced, this step introduced an alignment step to an otherwise self-aligned process. The development step did not significantly improve the DGW yield.

A second planarization technique is to physically grind off the polycrystalline material using polishers similar to those used to planarize the dielectric/metal stack in silicon CMOS processes. A sacrificial epitaxial layer can be grown at the top of the DGW epitaxy to protect the optical device from polycrystalline polishing residue. This technique may be useful for larger chips and full wafers.

The Gen. 2 chip demonstrated that DGWs could be created at Vitesse and successfully epitaxially grown. The Gen. 2 chip also had a variety of neural circuitry which was measured by A.C. Grot and was later used in Gen. 3-5 chip design.
Figure 4.5: Optical photograph of the Gen. 2 chip (2.4 mm × 2.4 mm) after pre-growth clean. Circuits with square bond pads (largest bond pads measure 100 μm × 100 μm) are around the perimeter of the chip and a single, large (1 mm × 1 mm) DGW is in the center of the chip. The DGW appears brighter than the rest of the chip because the exposed GaAs crystal at the bottom of the DGW reflects more light that the interlevel dielectric stack.
4.3 DGWs with Ohmic Contacts Chip (Gen. 3)

Two E-o-E optoelectronic integration DGW fabrication technique advances were tested and proved on the Gen. 3 (Vitesse HgAs2) chip (see Subsection 2.2.2). First, building on the DGW idea of the Gen. 2 chip, DGWs of various sizes were designed. This tested to see how small DGWs could be etched, cleaned and epitaxially grown. Second, in addition to having the DGWs etched at Vitesse, DGWs were source/drain ion-implanted and contacted with ohmic contacts. This addition provided an inherent bottom-side, n-type ohmic contact to epitaxially grown devices. Together these advances, namely small DGWs and inherent n-type contacts, provided indications as to the ultimate density of E-o-E based optoelectronic circuits. The Gen. 5 chip section (Section 4.5) further discusses large-scale and high-density E-o-E OEIC issues.

Figure 4.6 is an optical photograph of the Gen. 3 chip (3.5 mm × 3.5 mm) after pre-growth clean. Electronic circuits are scattered around DGWs of various sizes. DGWs appear brighter than the rest of the chip because the exposed GaAs crystal at the bottom of the DGWs reflects more light than the interlevel dielectric stack. Several rectangular (horizontally aligned long-axis) DGWs are near the bottom of the chip, a large DGW is in the center of the chip and a square DGW (500 μm × 500 μm) is above the right side of the large, central DGW. This square DGW, as well as most other DGWs on this chip, is S/D implanted and an ohmic contact - metal 1 - metal 2 - bond pad connection can be seen in the upper left corner of the DGW. Near the upper left corner of the 500 μm × 500 μm central DGW there is a cluster of small DGWs. Figure 4.7 is an enlarged optical photograph of this cluster of DGWs taken after DGW pre-growth clean, LED growth and polycrystalline material removal (using the procedures described in Sections 4.1 and 4.2). The DGWs sizes are: 100 μm × 100 μm, 40 μm × 40 μm, 30 μm × 30 μm, 20 μm × 20 μm (2 copies) and 10 μm × 10 μm (2 copies). All DGWs appeared to have good quality epitaxy except for one of the 10 μm × 10 μm DGWs, which turned out mostly polycrystalline, and the upper left corner of the 100 μm × 100 μm DGW, which has a macroscopic defect.
4.3. **DGWS WITH OHMIC CONTACTS CHIP (GEN. 3)**

This is believed to be due to poor pre-growth cleaning of minimum feature DGWs and not a fundamental MBE growth phenomenon because the other 10 μm × 10 μm DGW was single crystalline.

Figures 4.8-4.11 are optical photographs which show the LED fabrication process, in the central and surrounding DGWs, at four stages in the sequence. The LED fabrication sequence is detailed in Appendix A. Figure 4.8 shows the DGWs after LED growth and planarization, Figure 4.9 shows the DGWs after wet chemical mesa etch, Figure 4.10 shows the DGWs after silicon nitride deposition and Figure 4.11 shows the DGWs after via etch and n-type metal liftoff. All LEDs tested emitted light with characteristics nearly identical to those reported in Section 4.1. The additional series resistance can be calculated with typical ohmic contact resistances of ~0.3 Ω-mm and implant sheet resistances of ~200 Ω/□. The sheet resistance of the n-type epitaxial layers grown on the S/D implant must also be taken into account in this calculation.
Figure 4.6: Optical photograph of the Gen. 3 chip (3.5 mm × 3.5 mm) after pre-growth clean. Electronic circuits are scattered around DGWs of various sizes. DGWs appear brighter than the rest of the chip because the exposed GaAs crystal at the bottom of the DGWs reflect more light than the interlevel dielectric stack.
Figure 4.7: Optical photograph of Gen. 3 chip DGW cluster taken after DGW pre-growth clean, LED growth and polycrystalline material removal. The DGWs sizes are: 100 $\mu$m x 100 $\mu$m, 40 $\mu$m x 40 $\mu$m, 30 $\mu$m x 30 $\mu$m, 20 $\mu$m x 20 $\mu$m (2 copies) and 10 $\mu$m x 10 $\mu$m (2 copies).
Figure 4.8: Gen. 3 chip central DGW after LED growth and planarization.

Figure 4.9: Gen. 3 chip central DGW after wet chemical mesa etch.
4.3. *DGWS WITH OHMIC CONTACTS CHIP (GEN. 3)*

Figure 4.10: Gen. 3 chip central DGW after silicon nitride deposition.

Figure 4.11: Gen. 3 chip central DGW after via etch and n-type metal liftoff.
4.4 Winner-Take-All Circuit Chip (Gen. 4)

Another useful neural-inspired circuit is the winner-take-all (WTA) circuit. A WTA circuit consists of n identical units. In an optoelectronic circuit implementation, each unit consists of a photodetector, an emitter or modulator and analog circuitry. The unit which receives the largest optical input signal (P IN i) should be the only unit to emit or reflect light (P OUT i). In the present design an OPFET serves as the photodetector, an epitaxially grown LED serves as the emitter and two EFETs per unit compare signal intensities. A three-unit WTA circuit schematic is shown in Figure 4.12. This WTA circuit was designed and electrically simulated (SPICE) at Caltech [69], fabricated at Vitesse (HGAs3 through MOSIS), optoelectronically simulated (HSPICE simulations from layout-extracted OEIC with equivalent circuit models for LEDs and OPFETs) at MIT [123], MBE grown at MIT [123] and measured at Caltech [69]. This circuit was designed and fabricated using two advances which are important steps toward realizing higher levels of circuit integration. First, the WTA circuit was fully simulated using a layout extracted HSPICE circuit description and Vitesse model files, OPFET equivalent circuit models based on Gen. 1-3 measurements and empirical LED I-V and L-I characteristics. The simulated and measured WTA optical cross-over characteristics agree quite well. Second, E-o-E DGW fabrication advances developed with the Gen. 2 and Gen. 3 chips, namely layout-specified and S/D implanted DGWs with ohmic contacts, were used to demonstrate this three-unit WTA OEIC [133, 134, 135]. Together these advances should allow larger-scale and higher-density E-o-E based OEICs to be accurately designed and easily fabricated.

The WTA circuit shown in Figure 4.12 operates as a differential pair, but with three branches. The optical input intensity (e.g. P IN 2) is converted to a voltage (e.g. V2) by passing the OPFET photocurrent (e.g. I in 2) through a resistor (e.g. second branch sink EFET). V2 is the differential input voltage to the second branch differential EFET, which has an LED active load. For P IN 2 larger than P IN 1 and
Figure 4.12: Each unit of the 3-unit optoelectronic WTA circuit consists of an OPFET photodetector, an LED emitter and two EFETs (dimensions in W [μm]/L[μm]) [135].

P IN 3, V2 will be higher than V1 and V3. I out 2 will, therefore, be larger than I out 1 and I out 3 and, consequently, P OUT 2 will be greater than P OUT 1 and P OUT 3. Device sizing is based on HSPICE simulations and the geometries used for the three-unit WTA circuit are shown in Figure 4.12. WTA circuits can be scaled to an arbitrary number of branches.

This circuit was laid out using Mentor Graphics GDT software [136] and the circuit HSPICE [27] description was extracted based on Vitesse device and parasitic parameters available from MOSIS [26]. The circuit layout is shown in Figure 4.13. DCFL rail voltages (0.0 V and -2.0 V) are applied to the bond pads (far left), the current sink DFET is just to the right of the bond pads and two EFETs and an LED DGW, per unit, appear across the design. The OPFET was designed as a 40 μm × 1.2 μm EFET with a floating gate and LED equivalent circuits were not included in layout (DGWs indicate the final placement).

To complete the HSPICE circuit file, the OPFETs and LEDs were represented by equivalent circuits. The correspondence between EFET gate voltage and incident
Figure 4.13: 3-unit WTA circuit layout. DCFL rail voltages (0.0 V and -2.0 V) are applied to the bond pads (bottom), the current sink DFET is just above the bond pads and the two EfETs and the LED DGW, per unit, appear across the design.
Figure 4.14: I-V characteristic of two DFET diodes (3 μm × 2 μm) connected in series, forming the LED HSPICE model. Compare with LED I-V characteristic in Figure 3.35.

optical power, as described in Subsection 3.2.1 and summarized in Equation 3.8 (repeated below for convenience), was used to select an EFET $V_G$ range corresponding to typical input optical powers.

$$V_G = \frac{kT}{q} \ln \left( \frac{P_{\text{in}} \eta_o}{I_o} \right) \quad (4.2)$$

$P_{\text{in}}$ is expressed in units of Watts, $\eta_o \approx 340$ A/W and $I_o \approx 20$ nA. This relation gives gate voltages of 0.156 V and 0.186 V for incident optical powers of 30 nW and 100 nW, respectively. LEDs were represented in the HSPICE file by two DFET diodes (3 μm × 2 μm) connected in series. The I-V characteristic of this series pair is shown in Figure 4.14 and is nearly identical to the LED I-V characteristic shown in Figure 3.35. This electrical equivalent circuit combined with the 0.002 W/A LED slope efficiency, shown in Figure 3.36, formed the complete LED model.

The circuit was simulated with electrical biases representative of the operating
CHAPTER 4. E-O-E OEIC DEMONSTRATIONS

Figure 4.15: I-V characteristic of the currents through the three LEDs (LED 1, LED 2 and LED 3) versus the gate voltage on OPFET 2 for the 3-unit WTA circuit shown in Figure A.19

Figure 4.16: Simulated LED optical output powers versus OPFET 2 optical input power (30 nW on OPFET 1, 0 nW on OPFET 3).
optical powers, which ultimately were used to test the WTA circuit cross-over characteristics. OPFET 1, OPFET 2 and OPFET 3 gate voltages were set to 0.156 V, swept from 0.0 V to 0.186 V and set to 0.0 V, respectively. This represented optical input powers of $P_{IN\ 1} = 30\ \text{nW}$, $P_{IN\ 2} = 0-100\ \text{nW}$ and $P_{IN\ 3} = 0\ \text{nW}$. Figure 4.15 shows the I-V characteristic of the currents through the three LEDs (LED 1, LED 2 and LED 3) versus the gate voltage on OPFET 2. As expected, when the OPFET 2 gate voltage is less than the OPFET 1 gate voltage (i.e. 0.156) the LED 2 current is lower than the LED 1 current. The opposite is true when the OPFET 2 gate voltage is higher than the OPFET 1 gate voltage. LED 1 and LED 2 currents are equal when their respective OPFET gate voltages are equal. The LED 3 current is always low because its OPFET gate voltage is maintained at 0.0 V. This characteristic demonstrates the correct cross-over characteristic.

Figure 4.15 can be recast into an optical input power versus optical output power plot which is useful for comparison with measured data. Figure 4.16 shows the sim-
ulated optical output powers of the three LEDs (LED 1, LED 2 and LED 3) versus the simulated optical input power incident on OPFET 2. 30 nW and 0 nW of optical power were simulated to be incident on OPFET 1 and OPFET 3, respectively.

For comparison, the measured cross-over characteristic of the fully fabricated 3-unit WTA circuit is shown in Figure 4.17. 30 nW of optical power was applied to OPFET 1, the optical power was swept from 0 nW to 100 nW on the OPFET 2 and no optical power was applied to OPFET 3. The winning unit LED output power (P OUT 2) is greater than the other branches for input powers (P IN 2) greater than 30 nW, thus demonstrating the correct optoelectronic WTA circuit functionality. All possible input combinations functioned properly. The absolute input and output powers differ slightly between the simulated and measured characteristics. Possible reasons for these slight differences include OPFET responsivity and LED slope efficiency differences between the Gen. 4 devices and the model values which were based on Gen. 1-3 results. Optical power delivery and collection losses, due to light scattering and diffraction, also contribute to these differences. In general, however, there is good agreement between the simulated and measured WTA characteristics.

After the WTA circuit was simulated, the electronic portion of the WTA circuit was laid out (in a geometry compatible with the specific optical measurement apparatus) using standard Vitesse HGaAs3 design rules. The regions of the chip slated for LED growth were represented in the layout by specifying a dielectric growth window and a S/D n+ implant. DGWs were specified by stacking two standard etch mask layers: the passivation etch layer which cuts through the top overglass and the scribe-lane etch layer which cuts through interlevel-metal dielectric layers. To produce a near-vertical dielectric sidewall with CHF3/CF4/He reactive-ion etching (RIE), these layers were identically sized and aligned. The S/D n+ implanted region (typically 200 Ω/□) beneath the dielectric growth window region together with a standard ohmic contact (typically 0.3 Ω-mm) forms the bottom-side n ohmic contact. The design was fabricated at the foundry and returned unpackaged. Figure 4.18 is
Figure 4.18: Optical photograph of the Gen. 4 chip (3.5 mm × 3.5 mm). Electronic circuits and diagnostic cells are scattered around the chip. The 3-unit WTA circuit is in the upper right corner, just below and between the MOSIS and N38KAP lettering. Three 40 μm × 1 μm OPFETs surrounded by bond pads form the bulk of the circuit. The three 50 μm × 50 μm DGWs are just below the electronic portion of the circuit (DGWs appear brighter). The DGWs are relatively removed from the electronics for optical measurement convenience. Metal 1 lines connect the DGW ohmic contacts to the rest of the circuit.
Figure 4.19: Scanning electron micrograph (SEM) cross-section of a completed chip (MIT-OEIC-1 chip with LEDs for SEM convenience) after it was cleaved and the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ epitaxial layers were stained ($\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$) to appear brighter. The polycrystalline material deposited on the overglass is clearly visible (left) while single-crystalline material grows in the DGWs (right).

an optical photograph of the Gen. 4 chip (3.5 mm × 3.5 mm). Electronic circuits and diagnostic cells are scattered around the chip. The 3-unit WTA circuit is in the upper right corner, just below and between the MOSIS and N38KAP lettering. Three 40 $\mu$m × 1 $\mu$m OPFETs surrounded by bond pads form the bulk of the circuit. The three 50 $\mu$m × 50 $\mu$m DGWs are just below the electronic portion of the circuit (DGWs appear brighter). The DGWs are relatively removed from the electronics for optical measurement convenience. Metal 1 lines connect the DGW ohmic contacts to the rest of the circuit.

In preparation for growth, the S/D n$^+$ implanted GaAs at the bottom of the dielectric growth windows was cleaned. CF$_4$/O$_2$ RIE and an ultrasonic bath of buffered oxide etchant removed the residual material (a Teflon-like film) and dielectric at the bottom of the well. The chips were degreased and mounted with indium on a molyb-
denum block around the perimeter of a quarter wafer of bulk n$^+$ GaAs which served as a pyrometer source, RHEED crystal, and control sample. The block temperature was ramped at 15°C/min up to 600°C until the native oxide on the bulk GaAs desorbed. Five minutes later the native oxide in the dielectric growth windows on the chips was assumed to be desorbed. This is short enough to not significantly affect the MESFETs but it does impact the tungsten-plated aluminum interconnect metallization (see Subsection 3.1.1). Low-temperature hydrogen-plasma native oxide removal would be preferred. n$^+$ GaAs growth was initiated and the temperature was ramped to 530°C where the LED heterostructure was grown with a reduced As flux. The total growth thickness was 4.2 µm (4.5 hours) and approximately aligns the top surface of the single-crystalline GaAs with the top of the dielectric sidewalls. The heterostructure consisted of a 15 period n$^+$ Al$_{0.3}$Ga$_{0.7}$As(5 nm)/GaAs(5 nm) superlattice, 2.5 µm n$^+$ GaAs buffer, 0.3 µm n Al$_{0.3}$Ga$_{0.7}$As barrier, 0.6 µm p$^-$ GaAs active region, 0.7 µm p Al$_{0.3}$Ga$_{0.7}$As barrier, and a 0.1 µm p$^+$ GaAs contact. Single-crystalline material grows in the windows and polycrystalline material deposits on the top overglass and bond pads. Figure 4.19 is a scanning electron micrograph cross-section of the completed chip after it was cleaved and the Al$_{0.3}$Ga$_{0.7}$As epitaxial layers were stained (NH$_4$OH/H$_2$O$_2$). The polycrystalline material deposited on the overglass is clearly visible (left) while single-crystalline material grows in the DGWs (right).

After the chips were unloaded and the backside indium was stripped, the growth windows were photolithographically protected with photoresist (with a 5 µm overhang around the perimeter) and the polycrystalline material was wet etched with 1:1:5 H$_3$PO$_4$:H$_2$O$_2$:H$_2$O to expose the overglass and bond pads. The photoresist was then stripped resulting in a planar surface suitable for standard GaAs processing. To study the LED growth region a chip was cleaved, the Al$_{0.3}$Ga$_{0.7}$As layers were stained lighter (NH$_4$OH/H$_2$O$_2$) and a cross-sectional scanning electron micrograph was taken. Figure 4.20 shows that the top of the dielectric sidewall (far left) and the top of the LED heterostructure (far right) are in approximate alignment, that
Figure 4.20: Scanning electron micrograph (SEM) cross-section of a epitaxially grown chip (MIT-OEIC-1 chip with LEDs for SEM convenience) after it was cleaved and the Al$_{0.3}$Ga$_{0.7}$As epitaxial layers were stained (NH$_4$OH/H$_2$O$_2$) to appear brighter. The top of the dielectric sidewall (far left) and the top of the LED (far right) are in approximate alignment, the polycrystalline material has been successfully removed from the dielectric stack, and an approximately 5 μm wide transition region exists between the dielectric sidewall and good quality epitaxy.
Figure 4.21: 30° attack angle scanning electron micrograph (SEM) of an epitaxially grown and planarized chip (MIT-OEIC-1 chip with LEDs for SEM convenience) after it was cleaved at a 45° angle to the DGW, the Al₀.₃Ga₀.₇As epitaxial layers were stained (NH₄OH/H₂O₂) to appear brighter and the polycrystalline material has been successfully removed from the dielectric stack. The DGW and single-crystal material appear on the right and the DGW sidewall appears on the left. A thin (<1 μm) polycrystalline lip remains at the back DGW edge and the top dielectric layer (overglass) appears behind the lip, at the top-left of the SEM.
the polycrystalline material has been successfully removed from the dielectric stack
and that an approximately 5 \( \mu \text{m} \) wide transition region exists between the dielectric
sidewall and good quality epitaxy. Figure 4.21 is a 30° attack angle scanning electron
micrograph of the epitaxially grown and planarized Gen. 4 chip after it was cleaved,
the \( \text{Al}_{0.3}\text{Ga}_{0.7}\text{As} \) epitaxial layers were stained (\( \text{NH}_4\text{OH/H}_2\text{O}_2 \)) and the polycrystalline
material has been removed from the dielectric stack. A residual polycrystalline lip
appears to the left of the DGW indicating that the poly-strip mask was slightly mis-
aligned. Poly-strip alignment marks have been included on subsequent chip designs
to minimize misalignment (see Subsection 4.7.1).

After the chip was planarized, current-confining mesas were formed by a phospho-
ric acid based wet-etch, electrically insulating \( \text{Si}_3\text{N}_4 \) was chemical vapor deposited
(CVD) in 3 min. at 610°C (lower-temperature plasma enhanced CVD would be
preferred), and AuZn/Au p ohmic contacts were evaporated. A proton implanted an-
nular ring, resulting in high-resistivity material at the periphery of the epitaxial well,
would make the current-confining etch and dielectric deposition unnecessary thereby
simplifying processing and maintaining superior planarity.

Figure 4.22 is an optical picture of the 3-unit WTA circuit showing the three 40
\( \mu \text{m} \times 1 \mu \text{m} \) OPFETs surrounded by bond pads at the top, numerous MESFETs
and three 50 \( \mu \text{m} \times 50 \mu \text{m} \) DGWs with LEDs at the bottom. All electrical devices
on the chip function, but with some degradation (i.e. saturation current reduced by
10%) caused by long periods at temperatures in excess of 475°C. While no such shifts
would be present for growth temperatures below 475°C, these changes are predictable
and can be offset by proper design scaling (i.e. 10% gate width increase). I-V and
L-I curves from LEDs fabricated in the epitaxial wells and in the bulk control wafer
show no discernible differences (\( V_{TH} \) typically 1.2 V), as reported for previous LED
integrations. The efficiencies are also indistinguishable and are low (typically 0.01% 
at 100\( \mu \text{A} \) and 0.03% at 1mA) which is believed due to poor current confinement (see
Subsection 3.3.1).
Figure 4.22: Optical picture of the three-unit WTA circuit with three $40 \mu m \times 1 \mu m$ optical E-MESFETs surrounded by bond pads at the top and the three $50 \mu m \times 50 \mu m$ epitaxial growth wells with finished LEDs at the bottom.
Figure 4.23: Output EFET gate voltage transient response to a 280 Hz optical square wave applied to OPFET 2 (Branch 2). OPFET 1 (Branch 1) and OPFET 3 (Branch 3) optical input powers were held at 30 nW and 0 nW, respectively [70].

Figure 4.17 presented the measured WTA cross-over characteristics showing that the WTA circuit functions properly and agrees well with simulations. Figure 4.23 shows the output EFET gate voltage transient response to a 280 Hz optical square wave under the same measurement conditions previously discussed. The response time is presumably limited by the OPFET current. Figure 4.24 is a plot of a Gen. 4 LED optical output power versus time with a 5 mA constant current bias. No active cooling was provided. The output power drops by roughly 30% after 500 minutes of continuous operation. Possible causes for this decline include operation induced metallization annealing and defect propagation. LED lifetime requires further investigation and comparison with non-integrated LEDs.

By epitaxially growing LEDs on custom designed commercial VLSI GaAs MESFET integrated circuits with S/D n+ regions beneath foundry etched DGWs, a 3-unit optoelectronic winner-take-all circuit has been successfully simulated, fabricated and
Figure 4.24: Gen. 4 LED optical output power versus time with a 5 mA constant current bias [69].

demonstrated. With these integration advances, large-scale high-density E-o-E OE-ICs should now be possible [137, 138].
4.5 Winner-Take-All Array Chip (Gen. 5)

Building on the the E-o-E DGW fabrication and optoelectronic circuit design and simulation advances demonstrated with the 3-unit WTA circuit on the Gen. 4 chip, a larger-scale and higher-density OEIC was designed and fabricated on the Gen. 5 chip (HGAs3 through MOSIS). A 100-unit two-dimensional WTA circuit (10 × 10 array) was designed by A.C. Grot at Caltech [69], by generalizing the circuit to two-dimensions [138], and grown at MIT [123]. Similar to the 3-unit WTA, each unit of the 100-unit WTA has an OPFET detector (40 μm × 1 μm with 10μm S/D-to-gate spacing), a DGW for an epitaxial LED (30 μm × 30 μm) and two EFETs. The LED DGW is rotated by 45° to achieve two v-groove mesa sidewalls with a crystallographic wet etch (see Subsection 2.2.2). The area of each unit is approximately 100 μm × 100 μm and the total array area is roughly 1 mm × 1 mm, neglecting bond pads.

Figure 4.25 is a 50× optical photograph of the 100-unit WTA array before LED growth. OPFETs are squared with the array and the DGWs are rotated. The DGWs appear dark because the residual Teflon-like film has not yet been cleaned for growth. The EFETs are above (in-plane) each OPFET and are obscured from view by metal interconnect lines and power rails. Figure 4.26 is a 50× optical photograph of the 100-unit WTA array after pre-growth clean and LED growth. Single-crystalline LED material in DGWs appears bright and polycrystalline material appears dark. Roughly 5% of the DGWs (lower right corner of array) were presumably not cleaned sufficiently resulting in polycrystalline material in the DGWs. The new cleaning technique will presumably improve the DGW yield. LED structures have not yet been processed.

This array demonstrated that large-scale (>1 mm²) and high-density (< 100 μm × 100 μm pixel size) E-o-E OEICs should be possible. The ultimate size scale may be set by the epitaxial growth non-uniformity, further complicated by shadowing effects of the DGW sidewalls, while the ultimate density scale may be set by the minimum DGW size capable of supporting high quality epitaxy. Regions with only electrical or optical devices can exceed these size and density limitations.
Figure 4.25: 50× optical photograph of the 100-unit WTA array before LED growth. The total array size is approximately 1 mm².

Figure 4.26: 50× optical photograph of the 100-unit WTA array after LED growth. Single-crystalline LED material in DGWs appears bright and polycrystalline material appears dark.
4.6 Transmit/Receive Chip (MIT-OEIC-1,2)

Another important class of optoelectronic integrated circuits is high-speed single channel transmit and receive circuits (transceivers). Unlike the low-speed (KHz range) multiple-channel circuits demonstrated with the Gen. 1-5 chips, transceiver circuits should operate in the GHz range. Transceiver circuits are useful for digital optical networks, both fiber and free-space based, which typically operate at 1-10 Gb/s rates. These specifications require high-speed photodetectors, high-speed optical emitters or modulators and sophisticated circuit design. To explore transceiver OEICs, the GaAs circuit design expertise of Peter R. Nuytkens at MIT [75, 124] was combined with the E-o-E integration technique. As an historical note, the MIT-OEIC-(1,2) chip (HGaAs3 with only three interconnect metal levels and through MOSIS) with foundry etched ion-implanted DGWs and ohmic contacts was conceived, designed and fabricated before the first Caltech/MIT chip (Gen. 1).

To investigate E-o-E transmit and receive optoelectronic circuits, a generic transceiver circuit was designed [75]. Figure 4.27 shows the block diagram with ECL (-1.8 V, -0.8 V) and DCFL (-1.9 V, -1.4 V) level shifters for electrical input and output, an MSM photodetector with transimpedance amplifier for optical input, a laser diode (to be E-o-E integrated) or LED for optical output and a cross point switch to select the transceiver input-output mode. The electronic circuits were designed to operate at 1 Gb/s (roughly 2 GHz bandwidth) in the Vitesse HGaAs2 E/D MESFET process. The MSM detector was designed using standard gate metal fingers (see Subsection 3.2.2) and DGWs were designed for laser diodes (both in-plane and surface-emitting) and LED E-o-E integration. The DGWs were foundry etched, by stacking passivation and scribe lane etch layers, S/D ion-implanted and contacted with ohmic metal.

Figure 4.28 shows the layout of a single transceiver OEIC. It measures 400 \( \mu m \times 1500 \mu m \) and includes coplanar probable pads and two 400 \( \mu m \times 100 \mu m \) DGWs for laser diode or LED integration. The three top pads, each 100 \( \mu m \times 100 \mu m \) and read
Figure 4.27: Transceiver block diagram showing ECL and DCFL level shifters for electrical input and output, MSM photodetector with transimpedance amplifier for optical input, a monolithic laser diode or LED for optical output and a cross point switch to select transceiver function.

left to right, are ECL IN, GND and ECL OUT, respectively. A GND-Signal-GND coplanar probe can be used to deliver electrical drive signals and receive electrical output signals. The three pads on the left, read top to bottom, are VTT (-2.0 V lower DCFL rail), GND (0.0V upper DCFL rail) and BIAS, respectively. The bias pad is connected to the upper S/D ion-implanted DGW ohmic contact and can be used to bias the optical emitter in the off-state (discussed below). The 150 \( \mu \text{m} \times 100 \mu \text{m} \) DGW extensions on the left are for edge-emission. Designs with these extensions are placed along the edges of the chip and a saw can be used to cut through the extension revealing an emission face (e.g. IBAE laser laser facet). The pad below the upper DGW is for probing or bonding the optical emitter top contact, which is interconnected to this pad. The lower DGW will also receive an integrated optical emitter and is for diagnostic purposes only. The final two pads, on the right and read top to bottom, are the S0 and S1 cross-point switch select lines. A final observation of this layout is that the optical devices (laser or LED in DGW and MSM too small
to be seen in this figure) and the electrical circuits (dominated by bond pads) occupy similar areas [23].

Two other versions of the transceiver circuit, without cross-point switches, also appear on the chip. The second version routes the optical input to the electrical output and the electrical input to the optical output. The S0 and S1 pads are connected to MSM and laser current swing lines, respectively, instead. The third version is similar to the second version except that the laser current swing line is replaced by a transimpedance amplifier DFET (resistor) feedback gate control line. 24 transceiver circuits (8 copies of each of these three transceiver circuits) were placed across the 4.7 mm × 4.7 mm MIT-OEIC-1 chip. Figure 4.29 shows the circuit layout of the MIT-OEIC-1,2 chip with the 24 individual transceiver circuits and various diagnostic circuits in the scribe lanes. Vertical lines represent DGWs and solid black regions indicate bond pads. MIT-OEIC-2 is identical to MIT-OEIC-1, except for a corrected ring oscillator design, and was fabricated by MOSIS at no charge. Figure 4.30 is an optical photograph of the central 8 (of 24) transceiver OEICs on the MIT-OEIC-1 chip. Figure 4.31 is an optical photograph of an individual transceiver OEIC with the various functional regions labeled.
Figure 4.28: Layout of a single transceiver OEIC (400 μm × 1500 μm) which includes coplanar probable pads and two 400 μm × 100 μm DGWs for laser diode or LED integration. The 150 μm × 100 μm DGW extensions on the left are for edge-emission. The lower DGW is for diagnostic purposes only.
Figure 4.29: Circuit layout of MIT-OEIC-1,2 chip (4.7 mm × 4.7 mm) showing 24 individual transceiver circuits and various diagnostic circuits in the scribe lanes. Vertical lines represent DGWs and solid black regions indicate bond pads.
Figure 4.30: Optical photograph of the central 8 (of 24) transceiver OEICs on the MIT-OEIC-1 chip.
Figure 4.31: Optical photograph of an individual transceiver OEIC measuring 400 μm × 1500 μm, including coplanar probeable pads and two 400 μm × 100 μm DGWs for laser diode or LED integration.
To verify that the circuits were fabricated correctly, a version three transceiver circuit, with MSM bias and feedback DFET gate access, and an MSM with transimpedance amplifier were measured at DC. Both the electrical in to optical out and the optical in to electrical out modes were tested. In addition, characteristics were measured on chips as received from MOSIS/Vitesse as well as on chips that had IPSELs integrated with the E-o-E technique.

Figures 4.32 and 4.33 show the electrical input to optical output characteristics for transceivers directly from MOSIS/Vitesse and after IPSEL E-o-E integration (5 hours at 530°C), respectively. A 50 Ω resistor was connected between the laser bias (LB) pad, which is connected to the S/D DGW implant, and GND to mimic a laser diode. The current through this resistor appears on the vertical axis. The horizontal axis is the full range of ECL voltage levels which was applied to the ECL IN pad. VTT and GND were held at -2.0 V and 0.0 V respectively. Various resistors were connected between the LB and VTT pads to shift the output current curves. Figure 4.32 shows that a sharp transition, between the on and off currents, occurs at approximately -1.36 V. By decreasing the tunable resistor from infinity (no resistor) to 92 Ω, the on current ranges from 18.5 mA to 27 mA while the off current ranges from 3 mA to 15.5 mA. Figure 4.33 shows that for a fully integrated circuit under the same measurement conditions, a sharp transition occurs at approximately -1.24 V. The on current ranges from 15 mA to 23.3 mA while the off current ranges from 2.5 mA to 15.5 mA. Both characteristics show sharp transitions and sufficient current swing to drive laser diodes and LEDs. The difference in the characteristics is presumably due to an interconnect metal and ohmic contact resistance increase caused by the 530° MBE growth cycle. Reduced output currents are possibly due to rail voltages being divided across increased parasitic line resistances. 5 hour growths at 470°C should not show this degradation.

Figures 4.34 and 4.35 show the optical input to electrical output characteristics for the MSM with transimpedance amplifier circuit directly from MOSIS/Vitesse and
after IPSEL E-o-E integration (5 hours at 530°), respectively. This circuit outputs DCFL level signals and is identical to ones found in the transceiver cells. The circuit was tested by varying the feedback DFET (resistor) gate potential, to adjust the amplifier gain, while monitoring the T.I. amplifier output voltage and setting VTT and GND to -2.0 V and 0.0 V, respectively. Figure 4.34 shows the T.I. amplifier output voltage vs. DFET gate voltage characteristic for various incident optical powers. For DFET gate voltages in the range of -2.2 V to -2.7 V the circuit shows a strong photoresponse and for a DFET gate voltage ~ -2.5 V, the T.I. amplifier swings the full DCFL range. Figure 4.35 shows the same characteristic, but for the E-o-E integrated circuit. The characteristic has changed dramatically and appears to have shifted to higher output voltages by ~0.1 V and shifted to higher DFET gate voltages by ~0.5 V. The circuit does not swing the full DCFL levels (-1.8 V low instead of -1.9 V low). Such degradation is not expected for thermal cycles of 5 hours at 470°C.

These DC tests verified that the circuits are functional and capable of having LEDs and laser diodes E-o-E integrated. An important indication of circuit performance and thermal stability is high frequency performance. Preliminary high-speed measurements were conducted by P.R. Nuytkens at MIT which verified that the laser driver and MSM transimpedance amplifier circuits work to ~2 GHz [75]. A transceiver circuit with cross-over switch set to route the ECL input through the ECL to DCFL converter and back through the DCFL to ECL converter and on to the ECL output was measured on chips both with and without a 5 hour, 530°C thermal cycle. The circuit with no thermal cycle had a 0 dB mid-band gain and a 3 dB roll-off frequency of ~2 GHz while the circuit with the thermal cycle had a -10 dB mid-band gain and a 3 dB roll-off frequency of ~500 MHz. This gain and bandwidth reduction is presumably due to the increased interconnect and contact resistances which should not occur for 5 hour thermal cycles at 470°C. These circuits were bonded which could have added an additional resistive drop thereby decreasing the rail-rail voltage consistent with the observed reduced gain and bandwidth. Bond pad issues will be discussed in
4.6. TRANSMIT/RECEIVE CHIP (MIT-OEIC-1,2)

Section 5.3.
Figure 4.32: Laser driver current vs. ECL input voltage with various off-state bias resistors (pre-growth sequence).

Figure 4.33: Laser driver current vs. ECL input voltage with various off-state bias resistors (post-growth sequence, 5 hours at 530°C).
Figure 4.34: T.I. amplifier (with MSM photodetector) output voltage vs. DFET gate voltage characteristic with various incident optical powers (pre-growth sequence).

Figure 4.35: T.I. amplifier (with MSM photodetector) output voltage vs. DFET gate voltage characteristic with various incident optical powers (post-growth sequence, 5 hours at 530°C).
4.6.1 Integrated LEDs

LEDs were integrated on the transceiver chip (MIT-OEIC-1,2) using the E-o-E optoelectronic integration technique. The growth sequence was previously described in Sections 2.5 and 4.4, the LED heterostructure was presented in Figure 3.34 (a) and the process flow is detailed in Appendix A. Figure 4.36 was previously shown in Section 2.7 and is repeated here for convenience. Twenty LEDs were fabricated in this particular DGW, with a variety of top contact geometries, for diagnostic purposes. One LED top contact (p-type) is interconnected to the large bond pad below the DGW. The LED bottom contact (n-type) is made with a standard ohmic contact and is connected to the laser bias pad shown above the upper right corner of the DGW. Figure 4.37 is a 30° attack angle scanning electron micrograph of LEDs in DGWs (bottom and top), an aluminum bond pad (left) and the DGW sidewall top overglass layer (between DGWs and bond pads). The chip was cleaved through the lower DGW to provide a side view of the LED mesa. Metal p-type ohmic contacts can be seen on top of the right two LEDs in the bottom DGW and an annular ring contact and probe pad can be seen on the LED in the top DGW. The top of the LED heterostructure and the top of the dielectric sidewall are well aligned and the resulting surface is nearly planar (e.g. ≤ 1 μm ridges). A thin polycrystalline lip remains around the two lower DGW edges while no lip remains around the two upper DGW edges. This indicates that the poly-strip mask was slightly misaligned. Alignment marks for the poly-strip mask are included on the MIT-OEIC-3 chip.

The integrated LEDs were characterized by micro-probing the laser BIAS pad (upper left corner of Figure 4.36, which is connected to the bottom side n-type contact, and the top side p-contact of individual LEDs. The micro-probe tips were bent so that a Coherent model 212 calibrated power meter detector head could be brought to within 4 mm of the LED top surface. The detector has a \( \sim 1 \text{ cm}^2 \) silicon detector recessed \( \sim 1 \text{ cm} \) into the head. Since LEDs typically radiate in a \( \cos^2(\theta) \) pattern, it is estimated that most of the optical power emitted into the upper hemisphere was
Figure 4.36: Optical photograph of transceiver DGW with integrated LEDs. Figure 4.38 shows the layout of the mask used to fabricate these LEDs (Note: reflect about vertical axis to compare.).

Figure 4.37: 30° attack angle scanning electron micrograph of integrated LEDs.
Figure 4.38: Layout of LED mask (one DGW region) used to process integrated LEDs on the MIT-OEIC-(1,2) chips. Table 4.2 summarizes the LED geometries and optical characteristics of LEDs 1-6 which are labelled above. Relevant geometries are also indicated. LED 1-6 mesas are 30 μm x 30 μm and mesa trenches are 2.0 μm wide.

<table>
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<th>LED #</th>
<th>Drv. Cur. (mA)</th>
<th>Optical Power (nW)</th>
<th>Efficiency x10^-6 (W/A)</th>
<th>Con. Area (μm²)</th>
<th>Current Density (KA/cm²)</th>
<th>Mesa Size (μm²)</th>
<th>Via Size (μm²)</th>
<th>Min. Dist. Con.-Mesa (μm)</th>
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<td>900</td>
<td>26</td>
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<tr>
<td>2</td>
<td>1.0</td>
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<td>17.43</td>
<td>70</td>
<td>1.43</td>
<td>900</td>
<td>22</td>
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<tr>
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<td>1.0</td>
<td>21.20</td>
<td>21.20</td>
<td>60</td>
<td>1.67</td>
<td>900</td>
<td>18</td>
<td>6.0</td>
</tr>
<tr>
<td>4</td>
<td>1.0</td>
<td>19.51</td>
<td>19.51</td>
<td>50</td>
<td>2.00</td>
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<td>8.33</td>
<td>900</td>
<td>6</td>
<td>12.0</td>
</tr>
</tbody>
</table>

Table 4.2: Summary of the optical power, efficiency, contact area, current density (assuming no current spreading) and minimum distance from p-contact to etched mesa sidewall parameters for LEDs 1-6 under a constant 1 mA bias current.
collected. Within these experimental limits, I-V and optical power vs. current (I-I) characteristics were measured.

Figure 4.38 shows the layout of the LED mask (one DGW region) used to process integrated LEDs on the MIT-OEIC-(1,2) chips. Table 4.2 summarizes the LED geometries and optical characteristics of LEDs 1-6 (finger contact LEDs) which are labelled in Figure 4.38. Relevant geometries are also indicated. LED 1-6 mesas are 30 μm × 30 μm and the mesa trenches are 2.0 μm wide. The LED p-type contact size and location, and therefore current density and proximity to the wet-etched mesa trench sidewalls, respectively, varies within this LED series. Table 4.2 summarizes the optical power, efficiency, contact area, current density (assuming no current spreading) and minimum distance from p-contact to etched mesa sidewall parameters for LEDs 1-6 under a constant 1 mA bias current. It was observed that as the current density and the distance from p-contact to the etched mesa sidewall increased, so too did the optical output power and, therefore, the efficiency.

As discussed in Subsection 3.3.1, efficiency is expected to increase with current density. Efficiency is also expected to increase as the interface recombination velocity (s) decreases. For the case of LEDs 1-6, as the minimum distance from the p-contact to the mesa sidewall increases, the effective s decreases because less injected current spreads to the sidewalls where surface states are present. Log(I) vs. V plots for LEDs 1-6 show that the characteristic non-radiative current (∝ e^V/2kT) to radiative current (∝ e^V/kT) kink, occurring in the 10 nA range, is suppressed as the the p-contact to mesa spacing increases [139]. This indicates that while the increased efficiencies, progressing from LED 1 to 6, at 1 mA may be primarily due to increased current density, at lower currents the larger p-contact to mesa spacing increases efficiency. LEDs 11-16 are identical to LEDs 1-6 except that the p-contact to mesa edge distance is maintained. LEDs 11-16 serve as controls to determine the relative contribution of the increased current density and p-contact to mesa sidewall distance to the efficiency. LEDs 11-16 remain to be measured. Controls for determining the fraction of light
Figure 4.39: HP4145 parameter analyzer plot of the LED current (upper curve at low voltages), on the left vertical axis, and the optical output power (lower curve at high voltages), on the right vertical axis (1 V corresponds to 1 μW), as the ECL transceiver circuit input is swept from -1.8 V to -0.8 V. The transition occurs at an input voltage of \(\sim -1.25\) V.

LED 6 was the most efficient structure over the absolute current range of 1 nA to 1 mA. The relatively small efficiency, \(\sim 1 \times 10^4\) at 1 mA, can be increased by improving photon extraction and further confining the injected current to achieve even larger current densities. An (In,Ga)AsP LED structure, such as the one suggested in Subsection 3.3.1, should also perform significantly better due to its 470°C optimal growth temperature. (In,Ga)AsP LEDs for E-o-E integration are being actively pursued [47].

The final integrated transceiver-LED characterization performed was to drive an LED with the laser driver circuit. Though the LED threshold voltage was high (\(\sim 6\) V), presumably due to the degraded DGW ohmic contact caused by the 530°C growth, light modulation was observed. DCFL rail voltages (-2.0 V and 0.0 V) were applied to the transceiver circuit and a 7.5 V bias was applied to the p-contact of LED 4.
Figure 4.39 shows the LED current and optical output power as the ECL transceiver circuit input is swept from -1.8 V to -0.8 V. The current switches from \( \sim 4.34 \) mA to \( \sim 4.40 \) mA and the optical output power switches from \( \sim 704 \) nW to \( \sim 716 \) nW when the input crosses \( \sim -1.25 \) V. The optoelectronic circuit characteristics should improve with lower growth temperature integrated LEDs.

### 4.6.2 Integrated IPSELs

In-plane lasers and IPSELs were integrated on the transceiver chip using the E-o-E optoelectronic integration technique [140]. The growth sequence was previously described in Sections 2.5 and 4.4, the heterostructures and IPSEL fabrication technique were presented in Subsections 3.3.2 and 3.3.3, and the process flow is detailed in Appendix B. All IBAE etching and IPSEL processing was performed in collaboration with Dr. William D. Goodhue, Gerald D. Johnson and Dr. Joe P. Donnelly at MIT Lincoln Laboratory [91].

High quality quantum wells are essential for low-threshold laser diodes. Low-temperature photoluminescence measurements were performed on a control wafer and on an MIT-OEIC-1 transceiver chip. Four \( \text{In}_{0.2}\text{Ga}_{0.8}\text{As/GaAs} \) strained-layer quantum wells (\( \sim 30 \) Å, \( \sim 60 \) Å, \( \sim 80 \) Å and \( \sim 165 \) Å) were grown on a control wafer and on the chip at the same time. Figure 4.40 shows the photoluminescence intensity as a function of the material spontaneous emission wavelength. Because the argon-ion pump laser spot could not be focused down small enough to only illuminate the epitaxial material in a DGW, the intensities can not be compared. This is one possible explanation for why the two narrower quantum well (30 Å and 60 Å) peaks, which are less intense, were not observed from the chip material. The 30 sec. peak is perfectly aligned with the control wafer peak while the 60 sec. peak is not as intense as the control wafer peak. The peak positions and linewidths (though slits are wide) are nearly identical suggesting that the material in the DGW and on the control wafer are of similar quality.
Figure 4.41 is a scanning electron micrograph of a completed IPSEL in transceiver DGW. The waveguide is on the right and the end laser facet and parabolic mirror are in the middle. These structures were processed at the same time as the bulk epitaxial material presented in Subsection 3.3.3. Figure 4.42 is an optical photograph of the completed IPSEL-transceiver integration (shown before final metallization for clarity). IPSEL integration demonstrated that the top surface of the chip is planar enough, after IPSEL MBE growth and poly-strip, that features small enough for laser diode fabrication could be patterned with standard photolithography techniques using optical contact masks. 3.5 µm openings (parabola etch), 3.0 µm openings (via etch) and 4.0 µm lines (ridge waveguide etch) were all patterned with e-beam written optical contact masks and a high-resolution Karl Suss aligner [91]. Openings as small as 1.0 µm (laser facet etch) were opened in photoresist with a 4:1 projection aligner and a 4× e-beam written master mask.

Unfortunately, the final angled Ti/Au evaporation was fired in the wrong orientation and both end facets were Ti/Au coated. Time did not permit another fabrication sequence and therefore integrated IPSELs were not measured.
Figure 4.40: InGaAs MQW PL on bulk wafer and on transceiver chip.

Figure 4.41: Scanning electron micrograph of a completed IPSEL in transceiver DGW.
Figure 4.42: Optical photograph of the completed IPSEL-transceiver integration (shown before final metallization for clarity).
4.7 Multi-Epi Chip (MIT-OEIC-3 / NCIPT-OEVLSI-1)

The OEIC chips described in the previous six sections were designed for a single optical device, LEDs in the case of the Gen. 1-5 chips and IPSELS in the case of the MIT-OEIC-1,2 chip. These chips demonstrated that application-specific OEICs can be fabricated by designing an entire chip, with numerous and possibly autonomous sub-OEICs, for a given heterostructure and employing the E-o-E technique to integrate that particular epitaxial device [137]. It is also possible, however, to grow any one of a variety of heterostructures on a given chip. The MIT-OEIC-1,2 chip, for example, had LEDs grown and integrated on a few chips while other chips had IPSELS grown and integrated. The benefit of integrating several different optical devices, on different copies of a given chip, is that many OEICs can be characterized with a single electronic chip fabrication run. This reduces the overall fabrication time and reduces the development cost per OEIC. The drawback is that a given electronic circuit, which may be one of several resident on the chip, is typically designed for a particular optical device (e.g. a high-speed laser driver for IPSELS or a transimpedance amplifier for a long-wavelength MSM photodetector). If all electronic circuits on a chip are designed for the same optical device then, clearly, only that optical device should be integrated. Alternatively, if a few electronic circuits are designed to work with one optical device and a few electronic circuits are designed to work with a different optical device then, in this example, two optical device structures can be integrated with matched circuits. This is the concept of a multi-epi chip which can be generalized to arbitrary numbers of integrated heterostructures. Practical limitations to the number of different heterostructures a given chip should be designed to accommodate are that a MOSIS/Vitesse fabrication run typically returns ~100 chips and that as the number of different electrical-optical paired OEICs increases the fraction of fully functional OEICs on a chip decreases for a given heterostructure integration.
A multi-epi chip termed MIT-OEIC-3/NCIPT-OEIC-1 (HGaAs3 with four levels of interconnect metal and through MOSIS) was designed and fabricated to explore several OEICs with various heterostructures [58]. Process-, detector-, LED-, laser-, transceiver-, RTD-based SRAM-, SEED-, modulator- and thermal stability-related OEICs and diagnostic circuits are present on this chip. Tables 4.3 and 4.4 list the cell names and a description of all OEIC and diagnostic circuit cells on this chip. The page number provides a reference to the Sub-subsection overviewing each cell. A detailed description of all cells can be found in the “MIT-OEIC-3/NCIPT-OEVLSI-1 Optoelectronic VLSI GaAs Chip Design and Testing Manual” [58]. Figure 4.43 is a physical layout of the 4.7 mm × 4.7 mm chip and Figure 4.44 is an overlay of the cell outlines and names. This chip contains electronic circuit and DGW design contributions from several NCIPT member groups [125] and contributors will be referenced in the cell overview Sub-subsections which follow.

The MIT-OEIC-3/NCIPT-OEVLSI-1 chip was fabricated and received in March, 1995. Unfortunately several of the circuits were missing wires. The design was verified to be correct and the error was tracked to a Mentor Graphics GDT hierarchy flattening flag (-gdsmerge) problem. Instead of merging multiple abutting features into a single larger feature, this routine seemingly randomly removed what should have been the single feature. The error seems to only occur when there is a large number of constituent features to be merged and was not caught by visual inspection before fabrication. Flattening routines without this flag are now used.

All circuits were DC tested. All circuits which did not have wires deleted functioned as designed and these results are distributed throughout this document in the relevant sections. The circuits with missing wires are marked (*) in the summary tables (tables 4.3 and 4.4) and will be refabricated, along with new designs replacing the functional circuits, on the MIT-OEIC-4 chip (Section 4.8). DGW cleaning development, MBE growth, optical mask design and optical device processing is proceeding with the partially functioning chips. The MIT-OEIC-3/NCIPT-OEVLSI-1
lot was also split to test the effect of increased nitrogen concentration in the WN$_x$ barrier (see Subsection 3.1.1) beneath metal 4 on bond pads. This will be discussed in Section 5.3.
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Table 4.3: Part I: Cell name, description and page numbers of MIT-OEIC-3/NCIPT-OEIC-1 OEICs and diagnostic circuits.
### Table 4.4: Part II: Cell name, description and page numbers of MIT-OEIC-3/NCIPT-OEIC-1 OEICs and diagnostic circuits.

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<th>Cell Name</th>
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<td>Single element RTD SRAM cells w/o implanted DGWs. (* partial)</td>
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<td>SEED receiver fed into transmitter. (*)</td>
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<td>Standard D flip-flop.</td>
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<td>EB6 ring oscillator EFET and DFET.</td>
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Figure 4.43: MIT-OEIC-3/NCIPT-OEVLSI-1 chip layout (4.7 mm × 4.7 mm).
Figure 4.44: MIT-OEIC-3/NCIPT-OEVLSI-1 cell outlines and names. Numbers (1-13) indicate positions of FET Uniformity cells.
Figure 4.45: 200× optical photograph of the PCM RIE etch monitors (33-35), the Align Poly Strip cell (bottom left), the Align Upper Layers cell (bottom right) and part of the Stripe cell (upper left).

4.7.1 Process-Related Cells

PCM

PCM is a process control monitor bar which should be placed on all future E-o-E OEIC chips for qualification of discrete devices and integration process monitoring. The following electrical devices and structures are present: various EFETs; various DFETs; gate metal, metal 1, metal 2 and metal 3 resistor-snakes; source/drain implants-ohmic metal-metal 1, gate metal-metal 1, metal 1-metal 2 and metal 2-metal 3 contact strings; 5 μm × 50 μm and 20 μm × 5 μm S/D resistors (nominally 2 KΩ and 50 Ω, respectively); 100 μm × 5 μm, 100 μm × 10 μm, 100 μm × 5 μm with passivation and scribe lane cuts and 100 μm × 10 μm with passivation and scribe lane cuts TLMs; 80 μm × 80 μm passivation etch region (33), 80 μm × 80 μm passivation and scribe lane region (34) (i.e. DGW) and 80 μm × 80 μm scribe lane region (35) RIE etch monitors; and a 50 μm × 50 μm DGW between two pads which can be used
to test contact resistivities after all processing is complete. Figure 4.45 is an optical photograph of the RIE etch monitors 33-35 indicating that the scribe lane etch was very shallow. Most PCM structures were characterized both before and after MBE thermal cycles and the data are presented in Subsections 3.1.1 and 3.1.2.

**Fet Uniformity**

Fet Uniformity is a pair of representative inverter FETs (10 μm × 1.2 μm EFET, 2.8 μm × 3.4 μm DFET). This cell is present in 13 locations around the chip (see Figure 4.44) and serves as uniformity monitors useful for before and after MBE growth comparisons (see Subsection 3.1.3 for data).

**Backgate Reduction**

Backgate Reduction is a set of EFETs, DFETs and guard ring structures to characterize backgate sensitivity and backgate-effect reduction schemes. The following configurations are present: a 10 μm × 1.2 μm EFET and a 10 μm wide standard S/D-ohmic metal-metal 1 contact 20 μm below the EFET; a 10 μm × 1.2 μm EFET, a 10 μm wide standard S/D-ohmic metal-metal 1 contact located 20 μm below the EFET and four 10 μm wide standard S/D-ohmic metal-metal 1 contacts which form a ring around the EFET at a distance of 15 μm; a 2.8 μm × 3.4 μm DFET and a 10 μm wide standard S/D-ohmic metal-metal 1 contact located 20 μm below the DFET; and a 2.8 μm × 3.4 μm DFET, a 10 μm wide standard S/D-ohmic metal-metal 1 contact 20 μm below the EFET and four 10 μm wide standard S/D-ohmic metal-metal 1 contacts which form a ring around the DFET at a distance of 15 μm. Backgate voltages can be applied with a S/D contact (tap) while the depletion region under the guard ring, which can be extended with a positive voltage, can shield the FET from the backgate tap potential.
Align Poly Strip

Align Poly Strip includes structures for aligning the polycrystalline material strip mask to the chip. DGW plus signs with needle arms varying from 5 \( \mu \text{m} \) to 20 \( \mu \text{m} \) in width and squares of 10 \( \mu \text{m} \), 20 \( \mu \text{m} \), 30 \( \mu \text{m} \) and 40 \( \mu \text{m} \) edge lengths, are located across the chip. Figure 4.45 is an optical photograph of this cell. Single crystalline material will grow in these DGWs and will reflect more light than the surrounding polycrystalline material. These DGWs serve as alignment marks for polycrystalline material removal.

Align Upper Layers

Align Upper Layers includes alignment marks for masks beyond the polycrystalline strip mask. These masks typically need high resolution alignment marks which can only be written on or in DGW epitaxy. A 150 \( \mu \text{m} \times 100 \mu \text{m} \) DGW is included to provide space for writing alignment marks. The first mask beyond the polycrystalline strip mask, which typically writes the high resolution alignment marks, requires an alignment mark in the inter-DGW region. Plus signs in metal 3 are included for this purpose. Figure 4.45 is an optical photograph of this cell.

DGW Array

Well Array is a two-dimensional array of DGWs designed to explore the growth of devices in wells of various sizes, sidewall profiles and contact schemes. Figure 4.46 is an optical photograph of the 48 (6 rows \( \times \) 8 columns) element array. Each element contains a DGW, a S/D implant with ohmic contact connection to a horizontal rail (row) and a probe pad connected to a vertical rail (column) for top side connection. There are 14 (6+8) pads on left and lower edges of the array for wire bonding.

Each well has one of three possible variations: size (squares with 100 \( \mu \text{m} \), 75 \( \mu \text{m} \), 50 \( \mu \text{m} \), 40 \( \mu \text{m} \), 30 \( \mu \text{m} \), 20\( \mu \text{m} \), 10\( \mu \text{m} \) or 5\( \mu \text{m} \) sides); sidewall profile (scribe lane etch coincident with passivation etch or scribe lane etch outside passivation etch by + 2.0
4.7. MULTI-EPI CHIP (MIT-OEIC-3 / NCIPT-OEVLSI-1)

Figure 4.46: 50× optical photograph of the Well Array cell.

μm) and implant area (DGW 100% or roughly 25% S/D implanted). LEDs, RTDs, SEEDs or any other device with either two top side contacts or one top side contact and one n-type S/D bottom-side contact can be grown in this array of DGWs.

4.7.2 Detector-Related Cells

OPFET Array

OPFET ARRAY is a two-dimensional array of OPFET photodetectors designed to characterize OPFET geometry dependent responsivity, optical collection efficiency and frequency response. Figure 4.47 is an optical photograph of the 25 (5 rows × 5 columns) element array. Each OPFET has two possible variations: FET width (gate widths of 5 μm, 10 μm, 20 μm, 40 μm and 60 μm) and S/D-to-gate spacing (spaces of 2 μm, 4 μm, 8 μm, 16 μm, 32 μm). All gate lengths are 1.2 μm.
Figure 4.47: 200× optical photograph of the OPFET Array cell.

**OPFET Geometry**

OPFET Geometry consists of two annular ring OPFETs designed to characterize geometry dependent responsivity, optical collection efficiency and frequency response. Each annular ring OPFET is formed from four OPFETs positioned with gates along the four sizes of a square. One annular ring OPFET has two 25 μm × 1.2 μm OPFETs, two 20 μm × 1.2 μm OPFETs and a S/D-to-gate spacing of 15 μm. The other annular ring OPFET has two 45 μm × 1.2 μm OPFETs, two 20 μm × 1.2 μm OPFETs and a S/D-to-gate spacing of 24 μm.

**MSM Array**

MSM Array a two-dimensional array of 9 (3×3) Schottky gate metal based MSM photodetectors designed to characterize geometry dependent responsivity, optical collection efficiency and frequency response. Figure 4.48 is an optical photograph of the 9 (3×3) element array. Each MSM has 1.2 μm wide fingers, 2.0 μm spaces between
fingers and is square. The detectors have the following square side lengths: 6.4 \mu m, 12.8 \mu m, 19.2 \mu m, 25.6 \mu m, 32.0 \mu m, 38.4 \mu m, 44.8 \mu m, 51.2 \mu m and 57.6 \mu m.

**MSM T.I. Amp. Array**

MSM T.I. Amp. Array is a four element linear array of MSM photodetectors and associated transimpedance (T.I.) amplifiers. Figure 4.49 is an optical photograph of the array showing that the first and third elements (read left to right) include Schottky gate metal MSMs while the second and fourth elements contain DGWs for epitaxial MSMs. The T.I. amplifier was designed by P.R. Nuytkens at MIT [75].

Each T.I. amplifier has a DCFL output pad, a DFET feedback resistor gate pad and VTT and GND pads. The Schottky gate metal MSMs and DGWs measure 57.6 \mu m \times 57.6 \mu m and 110 \mu m \times 110 \mu m, respectively. Long-wavelength MSM detectors can be integrated in the DGWs and connected to the two 50 \mu m \times 50 \mu m T.I. amplifier input pads. The center-to-center detector spacing is 250 \mu m which is matched to fiber-ribbons.
Figure 4.49: 200× optical photograph of the MSM T.I. Array (top center), the bottom half of the Laser Array (top right), the full MSM Array (bottom right), the DCFL—ECL converter cell (bottom center), two PCM resistor snakes (bottom left) and the DC OE INV cell (left).

4.7.3 LED-Related Cells

LED Mirror

LED Mirror consists of two DGWs with staggered vias 1-3 and overlying metal 3 around one DGW. This metal ridge serves as angled mirrors, to collect LED optical side emission and redirect the light upward, as well as an optical shield to reduce the LED side optical emission coupled into the dielectric stack. Figure 4.50 is a schematic cross-section of a part of the LED Mirror cell showing the DGW (right) and stacked vias 1-3 and metal 3 angled sidewalls (left). The DGWs measure 60 μm × 60 μm and have S/D implants and ohmic metal contacts. One DGW does not have the angled mirrors and serves as a optical collection efficiency reference (control). A vertically stacked via 1-4 and ohmic metal - metal 4 (or 3) configuration can be used to provide an optical shield from the substrate to the top passivation (see Section 4.8).
EFET OE INV

EFET OE INV is an optical input to optical output non-inverting circuit. An OPFET (40 $\mu$m $\times$ 1.2 $\mu$m with 10 $\mu$m S/D-to-gate spacing) serves as an active load to a critically biased EFET (24 $\mu$m $\times$ 1.2 $\mu$m). The output of this optoelectronic inverter is connected to an EFET (84 $\mu$m $\times$ 1.2 $\mu$m) gate which has an LED (110 $\mu$m $\times$ 60 $\mu$m S/D implanted DGW) active load. The LED is 200 $\mu$m from the OPFET to reduce positive optical feedback. A S/D ohmic contact guard ring around the OPFET and two S/D backgate contacts at different distances (10 $\mu$m and 30 $\mu$m) from the guard ring are present to test the circuit sensitivity to backgating. The OPFET gate can be contacted to control the OPFET sensitivity.

The input EFET gate potential and the optical power on the OPFET determine the optoelectronic inverter characteristic. The advantage of this design is that the OE inverter can be tuned to particular input optical power ranges, but the drawback is that an additional bias line (input EFET gate) is required.
CHAPTER 4. E-O-E OEIC DEMONSTRATIONS

DFET OE INV

DFET OE INV is an optical input to optical output inverting circuit. An OPFET (40 $\mu$m × 1.2 $\mu$m with 10 $\mu$m S/D-to-gate spacing) serves as a pull-down EFET and, together with a DFET (6 $\mu$m × 8 $\mu$m) active load, forms an optoelectronic inverter. The output of this OE inverter is connected to a DFET (50 $\mu$m × 1.2 $\mu$m) gate which has an LED (110 $\mu$m × 60 $\mu$m S/D implanted DGW) active load. Since the OPFET source is at the lowest potential of the circuit backgating effects should be minimized. The LED is 200 $\mu$m from the OPFET to reduce positive optical feedback. A S/D ohmic contact guard ring around the OPFET and two S/D backgate contacts at different distances (10 $\mu$m and 30 $\mu$m) from the guard ring are present to test the circuit sensitivity to backgating. The OPFET gate can be contacted to control the OPFET sensitivity.

The advantage of this design is that a DFET is used to power the LED and since the saturation current of a DFET is roughly four times greater than that of a similarly sized EFET, this DFET can be compact. The drawback to this design is that an additional power line, -3.0 V or lower with standard -2.0 and 0.0 DCFL rails, connected to the OPFET source is required for the DFET to be turned off by the optoelectronic inverter output. This additional power line is both inconvenient and can increase backgating effects (see Section 5.2).

DCFL OE INV

DCFL OE INV is an optical input to optical output inverting circuit. An OPFET (40 $\mu$m × 1.2 $\mu$m with 10 $\mu$m S/D-to-gate spacing) serves as a pull-down EFET and, together with a DFET (6 $\mu$m × 8) active load, forms an optoelectronic inverter. The output of this optical-electrical inverter is connected to an EFET (84 $\mu$m × 1.2 $\mu$m) gate which has an LED (110 $\mu$m × 60 $\mu$m S/D implanted DGW) active load. The LED is 200 $\mu$m from the OPFET to reduce positive optical feedback. A S/D implant guard ring around the OPFET and two S/D backgate contacts at different distances
(10 μm and 30 μm) from the guard ring are present to test the circuit sensitivity to backgating. The OPFET gate can be contacted to control the OPFET sensitivity.

The advantage of this design is that no additional critical bias or power lines are required, as opposed to the EFET OE INV and DFET OE INV circuits, though the optical power operating ranges are not 

### 4.7.4 Laser-Related Cells

**Laser and Driver**

Laser and Driver is a high-speed DCFL input to laser diode current driver circuit designed by P.R. Nuytkens at MIT[75]. Figure 4.51 is a schematic diagram of this circuit. A DCFL input signal causes the output of the current mirror to swing 4I where I is the current through the resistor above node 5. The current I, and therefore 4I, can be adjusted by externally injecting current into node 5. This sets the current swing of the laser driver. The off-state current through the laser diode can be adjusted by connecting an external resistor to node 6, which will add in parallel to an 800 Ω
Figure 4.52: Layout extracted HSPICE simulation of DCFL input (top panel) to laser current output (bottom panel).

on-chip resistor. The minimum off-state current is \( \sim 2 \) mA. Figure 4.52 is a layout extracted HSPICE simulation and shows the circuit response to a 1 ns period DCFL input signal. The Laser and Driver cell consists of two versions of this circuit, one positioned next to a S/D implanted 500 \( \mu \text{m} \times 100 \mu \text{m} \) laser diode DGW and the other next to a non-implanted laser diode DGW. The layout of this cell is similar to the MIT-OEIC-1,2 transceiver design.

**Laser Array**

Laser Array is a linear array of laser DGWs, with various contact schemes, and co-planar probe pads designed to characterize edge-emitting and in-plane surface-emitting lasers from DC to microwave frequencies. Figure 4.49 is an optical photograph of the bottom half of the Laser Array cell. The 6 (6 rows \( \times \) 1 column) element array has three S/D implanted laser diode DGWs and three non-implanted laser diode DGWs. Each 500 \( \mu \text{m} \times 60 \mu \text{m} \) DGW has three associated bond pads intended for
either GSG cascade probes, in the case of a two terminal laser the outer pads are GND and the middle pad is for the p-type up signal, or SGS cascade probe, in the case of a three terminal laser where one S-G is used for current biasing and the extra S is for the voltage signal. SGS probes can only be used for the non-S/D implanted wells since the outer pads are tied together in metal 1. The DGWs extend 150 μm beyond this well so that a saw can be used to cut the chip (laser mirrors cut with RIE or IBAE) and allow an edge-emitting laser to fire off of the side of the chip.

**VCRO**

VCRO is a voltage-controlled frequency tunable ring oscillator serving as a voltage tunable high-speed DCFL source. The ring oscillator has seven inverter stages (10 μm × 1.2 μm EFETs and 2.8 μm × 3.4 μm DFETs) and “current-starving” EFETs (30 μm × 1.2 μm) between the inverter EFETs and GND. A push-pull output (10 μm × 1.2 μm EFET and 2.8 μm × 3.4 μm DFET) drives a two stage output (stage one: 30 μm × 1.2 μm EFET and 7 μm × 3 μm DFET, stage two: 70 μm × 1.2 μm EFET and 18 μm × 3 μm DFET). The propagation delay time per stage is tunable from 150 ps to 110 ps for a frequency-tuning-voltage varying from 0.4 V to 0.6 V. DCFL signals are therefore nominally tunable from 475 MHz to 650 MHz. Performance estimates are based on layout extracted HSPICE simulations.

**Optical Clock**

Optical Clock is a voltage tunable optical pulse train circuit. The VCRO cell was combined with the Laser and Driver cell, which consists of a high-speed laser diode drive circuit and laser diode DGW, to form a circuit capable of generating a 50% duty cycle optical clock at frequencies between 475 MHz and 650 MHz.

**MWAVEDEV**
Figure 4.53: 200× optical photograph of MWAVWDEV cell (top right) and ORODERED1 transceiver cell (left). Upper left corner of the Well Array cell appears in the lower right corner.

MWAVWDEV contains a variety of active devices for microwave performance characterization. A 10 \( \mu m \times 1.2 \mu m \) EFET, a 90 \( \mu m \times 1.2 \mu m \) EFET, a 10 \( \mu m \times 3.6 \mu m \) DFET and a 40 \( \mu m \times 3.6 \mu m \) DFET are connected to associated co-planar GSG probe pads. Figure 4.53 is an optical photograph of this cell.

MWAVEDUM

MWAVEDUM contains devices for microwave setup calibration and characterization. A variety of GSG—GSG short and open combinations and device parasitic extraction structures (e.g. all-but-channel FET's) are included.
4.7.5 Transceiver-Related Cells

ORODRED1

ORODRED1 is identical to the MIT-OEIC-1,2 transceiver circuit, version 1, described in Section 4.6. It was fabricated again to characterize the high-frequency performance differences between the Vitesse HGaAs2 process (MIT-OEIC-1,2) and the HGaAs3 process (MIT-OEIC-3/NCIPT-OEVLSI-1). Figure 4.53 is an optical photograph of this cell and shows the long vertical saw lane DGW used to access in-plane emitting laser facets.

ORODRED2

ORODRED2 is identical to the MIT-OEIC-1,2 transceiver circuit, version 2, described in Section 4.6. It was fabricated again to characterize the high-frequency performance differences between the Vitesse HGaAs2 process (MIT-OEIC-1,2) and the HGaAs3 process (MIT-OEIC-3/NCIPT-OEVLSI-1).

ORODRED3

ORODRED3 is identical to the MIT-OEIC-1,2 transceiver circuit, version 3, described in Section 4.6. It was fabricated again to characterize the high-frequency performance differences between the Vitesse HGaAs2 process (MIT-OEIC-1,2) and the HGaAs3 process (MIT-OEIC-3/NCIPT-OEVLSI-1).

ECL-DCFL

ECL-DCFL is a level shifting circuit for converting ECL signals (-1.8 V, -0.8 V) to DCFL signals (-1.9 V, -1.4 V) and was designed by P.R. Nuytkens at MIT [75]. The circuit schematic is shown in Figure 4.54 and layout extracted HSPICE simulations are presented in Figure 4.55 for a 1 ns period ECL input wave.
Figure 4.54: Circuit schematic of the ECL-DCFL level shifting circuit.

Figure 4.55: Layout extracted simulated performance of the ECL-DCFL circuit. DCFL output waves (top panel) and rail currents (bottom panel) are shown for a 1 ns period ECL input wave.
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Figure 4.56: Circuit schematic of the DCFL-ECL level shifting circuit.

**DCFL-ECL**

DCFL-ECL is a level shifting circuit for converting DCFL signals (-1.9 V, -1.4 V) to ECL signals (-1.8 V, -0.8 V) and was designed by P.R. Nuytkens at MIT [75]. The circuit schematic is shown in Figure 4.56 and layout extracted HSPICE simulations are presented in Figure 4.57 for a 1 ns period DCFL input wave.

**ESD Prot**

ESD is an electrostatic diode shock protection circuit designed by P.R. Nuytkens at MIT [75]. The ESD circuit consists of two diode configured DFETs connected in series between the DCFL rails such that both are reverse biased. Input and output signals are connected to the node between the diodes. One of the two diodes will become forward biased, and therefore clamp the voltage, if the input or output signal exceeds $V_T$ above 0.0 V or $V_f$ below -2.0 V. This protects the circuit from high voltage electrostatic shocks. This circuit was layout extracted HSPICE simulated,
Figure 4.57: Layout extracted simulated performance of the DCFL-ECL circuit. ECL output waves (top panel) and rail currents (bottom panel) are shown for a 1 ns period DCFL input wave.

and shown to work, with a 1 ns period ECL signal.

**Laser Driver**

Laser Driver is the circuit described in the Laser and Driver Sub-subsection in Subsection 4.7.4. The electronic circuit portion was repeated in this cell, with additional probe pads, for DC and low frequency characterization with hybrid bonded laser diodes.
Figure 4.58: 200× optical photograph of the MEM Array cell.

4.7.6 RTD SRAM-Related Cells

RTD-based static random access memory (SRAM) related cells were designed by R.J. Aggarwal at MIT [63] and were layed out as part of the MIT-OEIC-3/NCIPT-OEVLSI-1 chip [141]. These basic cells were designed to evaluate the E-o-E integration technique for use in fabricating low-power high-speed memory arrays [61].

MEM Array

MEM Array is a four bit RTD-based SRAM memory array. It is designed to study basic RTD memory architecture issues and E-o-E integration density issues such as the effects of RTD non-uniformity on SRAM performance [61]. Figure 4.58 is an optical photograph of the MEM Array cell, showing four central RTD DGWs, write and read decode circuitry to the left and right of the DGWs, respectively, and nine bond bands for power, select and data lines.

MEM Array is composed of four identical RTD memory cells. Each cell is composed of a WRITE EFET (240 μm × 1.2 μm), a READ EFET (240 μm × 1.2 μm) and a S/D implanted RTD DGW (100 μm × 100 μm). Write and read EFET drains
Figure 4.59: Circuit schematic of MEM Array circuit [63, 58].

are connected to the implant which provides the interconnection between the EFETs and the RTDs. The read and write operations have separate input and output circuitry and each has two select lines, S0 WRITE/READ and S1 WRITE/READ, to choose one of the four memory cells. There also a single WRITE BUS, a single READ BUS and three power lines (VRTD, VTT and GND). Figure 4.59 is a circuit schematic of the MEM Array circuit. Figure 4.60 shows the layout extracted HSPICE read/write simulation of two of the four memory bits. This simulation was performed by R.J. Aggarwal at MIT [63], using experimental RTD I-V curves, and shows correct operation.

MEMDC

MEMDC is a series of single bit RTD-based SRAM cells. These cells are designed to study the effects of RTD parameters such as size, doping, and peak-to-valley current and voltage ratios on the basic operation of the SRAM. Each cell is composed of a WRITE EFET (240 μm × 1.2 μm or 84 μm × 1.2 μm), a READ EFET (240 μm ×
Figure 4.60: Layout extracted HSPICE simulated performance of MEM Array 00 and 11 bits. Panel 1 shows the Select line and Data line. Panel 2 shows the voltage at the 11 bit Storage node. Panel 3 shows the Read bus voltage and the 11 bit Read Select line. Panel 4 shows the voltage at the 00 bit storage node. Panel 5 shows the Read bus voltage and the 00 bit Read Select line [63, 58].
Figure 4.61: Circuit schematic of the SEED REC cell. SEED2 photocurrent raises the node 5 potential while SEED1 photocurrent decreases the node 5 potential. The intensity ratio determines the steady-state node 5 voltage. (Extra inverter for simulation only) [142, 58].

1.2 μm or 84 μm × 1.2 μm) and an RTD DGW (100 μm × 100 μm). The FETs and RTDs are connected and operated similarly to single bits in the MEM Array cell.

MEMDC Noimp

MEMDC Noimp is identical to MEMDC except that the RTD DGWs are not S/D implanted. EFET to RTD connections are made through an extra top-side contact. Together, MEMDC Noimp and MEMDC will explore the effect of S/D implanted DGWs on RTD performance.

4.7.7 SEED-Related Cells

The SEED/MQW modulator related cells were designed in collaboration with Dr. Charlie Kuznia at USC [142]. These basic cells were designed to evaluate the E-o-E
Figure 4.62: Circuit schematic of the SEED TRANS cell. The DCFL input at node 2 causes a large voltage swing on node 6. The state of optical intensity modulators SEEDOUT1 and SEEDOUT2 are read with a pair of optical beams to produce a dual-rail optical signal [142, 58].

optoelectronic integration technique for use in fabricating FET-SEED OEICs [15].

SEED REC

SEED REC is a circuit that converts an intensity coded dual-rail optical signal to an electrical DCFL signal. The dual-rail optical signal enters the circuit through two 20 $\mu$m by 20 $\mu$m SEED heterostructure p-i-n diodes fabricated in DGWs on 80 $\mu$m centers as shown in the circuit schematic in Figure 4.61. The center node of the two series connected SEEDs is connected to the EFET gate of a DCFL inverter (10 $\mu$m $\times$ 1.2 $\mu$m EFET and 3.4 $\mu$m $\times$ 2.8 $\mu$m DFET). If the optical intensity incident on SEED1 is larger than that incident on SEED2, a DCFL high signal will result. Similarly, reversing the intensities will result in a DCFL low.
SEED NOR

SEED NOR is a two-input NOR gate consisting of a DCFL inverter with the EFET replaced by two parallel input EFETs. This cell represents arbitrary electronic logic necessary for FET-SEED circuits. This cell is used in the SEED RECNORTANS cell.

SEED TRANS

SEED TRANS converts a DCFL signal to a higher voltage signal required for driving SEED modulators. A DCFL input signal is amplified with the HIGHV2 circuit (see the HIGHV2 Sub-subsection in Subsection 4.7.8) to produce a 0 to ~8.5 V swing which is, in turn, connected to the common node of two serially-connected output SEED pin diodes. This voltage swing generates complementary voltages across the SEEDs, setting the two SEEDs in complementary absorption states. At the proper wavelength, a high voltage gives high absorption in the SEED. The SEED states are read out by reflecting a pair of optical beams from the two 20 μm × 20 μm SEED windows on 80 μm centers. Figure 4.62 is a circuit schematic of this circuit.

SEED RECTRANS

SEED RECTRANS connects the SEED REC circuit to the SEED TRANS circuit to form and optical inverter. This circuit receives a dual-rail optical signal, complements it, and sets the SEED modulators accordingly for optical readout. The optical signal enters SEED1 and SEED2 and sets the modulators SEEDOUT1 and SEEDOUT2 as shown in the Figure 4.63 circuit schematic.

SEED RECNORTANS

SEED RECNORTANS connects two SEED REC circuits to a SEED NOR circuit and on to a SEED TRANS circuit to produce a two-input NOR gate with optical inputs and outputs. Two dual-rail optical signals enter the circuit and set the state of
Figure 4.63: Circuit schematic of the SEED RECTRANS cell. Optical dual-rail signals on SEED1 and SEED2 create a small voltage swing at node 7. The circuit complements and amplifies this voltage to produce a large voltage swing at node 9. The voltage at node 9 sets the state of modulators SEEDOUT1 and SEEDOUT2 [142, 58].
two SEED modulators according to the logical NOR function. Figure 4.64 shows the circuit schematic and Figure 4.65 presents the layout extracted HSPICE simulation of this cell. Figure 4.66 is an optical photograph of this cell.

\section*{D FLIP FLOP}

D FLIP FLOP is a DCFL D-type flip flop electrical circuit with clock and data inputs and Q and \bar{Q} outputs. The design was provided by Vitesse [28]. D-type flip flops are useful for shift register circuits. Optoelectronic shift registers are typically required
Figure 4.65: Layout extracted HSPICE simulation of the SEED RECNORTANS circuit. The current source I(seed2a) alternates between 0 and 10 microamps every 2 microseconds. The current source I(seed2b) alternates every 4 microseconds (shown as the thick dashed line). The voltage for the SEED modulators is low only when both I(seed2a) and I(seed2b) are both high. The bottom graph is the output voltage with I(seed1a) high and I(seed2a) swept from 0 to 10 microamps [142, 58].
for optical processing circuits.

4.7.8 Modulator-Related Cells

In-plane modulator and waveguide related circuits were designed by Y. Royter at MIT [143] and were laid out as part of the MIT-OEIC-3/NCIPT-OEVLSI-1 chip [144]. These basic cells were designed to evaluate the E-o-E integration technique for use in fabricating in-plane modulator and waveguide based photonic integrated circuits. The HIGHV2 circuit was also employed in the SEED TRANS circuit (see SEED TRANS Sub-subsection in Subsection 4.7.7).

HIGHV1

HIGHV1 is a DCFL input in-plane modulator driver circuit capable of 0.1 V to 8.5 V output swings without exceeding MESFET breakdown voltages (e.g. $V_{DG} \approx 5$ V). 4.5 V, 9.0 V and 0.0 V rails are required and reverse biased modulator capacitive
loads up to 1 pF can be driven at switching speeds up to 200 Mbits/s while supplying \(~1\) mA of direct current. The driver output terminals are not referenced to ground. The circuit consists of two groups of FETs, those with source nodes at \(~4.5\) V and those with source nodes at 0.0 V. Both groups are surrounded by S/D-ohmic metal guard rings which can be contacted to isolate and control the substrate potential (see Section 5.2). This circuit will contribute to the characterization of this backgate guard ring technology.

Figure 4.67 is an optical photograph of the HIGHV1 cell. It is located next to the Stripe diagonal DGW cell, in which in-plane modulator heterostructures can be fabricated. The circuit output pads (30 \(\mu\)m \(\times\) 30 \(\mu\)m) and modulator can be interconnected (i.e. metal 5) to complete fabrication. A 500\(\mu\)m long modulator and drive circuitry can be isolated from the rest of the chip by cleaving along the thin DGWs perpendicular to the main Stripe diagonal (see Subsection 2.2.2 for crystal orientation and the Stripe Sub-subsection for DGW dimensions). This is a convenient technique
HIGHV2

HIGHV2 is a DCFL input SEED modulator driver circuit capable of 0.2 V to ~9.0 V output swings without exceeding MESFET breakdown voltages (e.g. $V_{DG} \approx 5$ V). 4.5 V, 9.0 V and 0.0 V rails are required and reverse biased SEED capacitive loads up to 0.1 pF, typical of 20 $\mu$m $\times$ 20 $\mu$m SEED devices, can be driven at switching speeds up to 100 Mbits/s while supplying $\sim$5 $\mu$A of direct current. The driver output terminals are referenced to ground and no backgate protection is included. Figure 4.68 is a circuit schematic of this cell and Figure 4.69 is the layout extracted HSPICE DC transfer curve and AC simulation of this circuit. This circuit is located close to DGWs and can be interconnected (i.e. metal 5) to SEED modulators.
LOWV

LOWV is a DCFL input low-voltage modulator driver circuit capable of DCFL rail voltage swings. DCFL rail voltages, or rail voltages up to the MESFET $V_{DG}$ breakdown limit (~5 V), are required and modulator capacitive loads up to 1 pF can be driven at switching speeds of up to 300 Mbits/s. The output terminals are referenced to ground and the circuit is a simple DCFL super-buffer.

T.I. MOD

T.I. MOD is the transimpedance amplifier without associated Schottky gate based MSM detector, as discussed in the T.I. Array Sub-subsection of Subsection 4.7.2, and is positioned next to the Stripe diagonal DGW. In-plane modulators can be biased as in-plane detectors and the T.I. MOD can amplify the detector photocurrents.
Figure 4.70: Layout of the Stripe cell showing (1) the long modulator DGW (lower left to upper right), (2) the thin cleave guide DGW (upper right corner and perpendicular to the modulator DGW) and (3) saw lane DGWs (left and right edges).

**Stripe**

Stripe is a collection of large area DGWs. The first DGW is a long (6.64 mm), thin (400 µm) DGW oriented at a 45° angle which spans the entire chip as shown in Figure 4.67. The layout of the Stripe cell is shown in Figure 4.70. This DGW is useful for in-plane modulators, modulator/detector/waveguide optical circuits such as Mach-Zehnder interferometers, broad area lasers and characterizing a large number of smaller devices such as RTDs and LEDs. The DGW is along the 011 crystal direction (see Subsection 2.2.2 for crystal orientation). A 60µm wide S/D implant is present along both sides to provide bottom-side n-type contact. The entire DGW does not need to be implanted if the first epitaxial layer grown is n+ doped.

A second DGW in the Stripe cell is perpendicular to the main stripe, also shown in Figure 4.67. This DGW is 50 µm wide and is located 920 µm (along edges of the chip) from the upper right corner of the chip. 500 µm to 700 µm long in-plane modulators can be isolated from the rest of the chip by cleaving along this DGW and
through the triangular DGW in the corner of the chip.

The final DGWs are located along the left and right edges of the chip. These 150 
\( \mu \text{m} \) wide, 4.7 mm long DGWs provide saw lanes for removing the edge of the chip to 
expose RIE or IBAE defined laser mirror facets for edge emission. Small gaps in these 
DGWs exist to electrically isolate the epitaxial material grown in the laser DGWs 
along the chip edge.

### 4.7.9 Thermal Stability-Related Cells

Thermal stability-related cells were designed in collaboration with E.K. Braun at 
MIT [55] and were layed out as part of the MIT-OEIC-3/NCIPT-OEVLSI-1 chip 
[145]. These cells were designed to extend the characterization of the Vitesse HGaAs3 
process. In particular, cells were designed to determine the role of the via 1 to 
ohmic metal edge spacing in thermal degradation and to test alternate ohmic contact 
schemes. Results of these tests were presented in Subsections 3.1.1 and 3.1.2 [57].

**Array4 x 1.4 (EB1)**

Array4 x 1.4 is a contact string with 304 metal 1-ohmic metal-S/D implant contacts 
with M1 interconnect metal. The ohmic metal is 4.0 \( \mu \text{m} \) x 4.0 \( \mu \text{m} \) and the via 1 is 1.4 
\( \mu \text{m} \) x 1.4 \( \mu \text{m} \) (centered). The implant resistor dimensions are 2.0 \( \mu \text{m} \) long and 6.0
μm wide. This cell was designed to extract the ohmic contact resistance dependence on the ohmic contact size and via 1 size. Figure 4.71 is a diagram of the contact geometry.

**Array4×3.0 (EB2)**

Array4×3.0 is a contact string with 304 metal 1-ohmic metal-S/D implant contacts with metal 1 interconnect metal. The ohmic metal is 4.0 μm × 4.0 μm and the via 1 is 3.0 μm × 3.0 μm (centered). The implant resistor dimensions are 2.0 μm long and 6.0 μm wide. This cell was designed to extract the ohmic contact resistance dependence on the ohmic contact size and via 1 size. Figure 4.72 is a diagram of the contact geometry.

**Array2×1.4 (EB3)**

Array2×1.4 is a contact string with 304 metal 1-ohmic metal-S/D implant contacts with metal 1 interconnect metal. The ohmic metal is 2.0 μm × 2.0 μm and the via 1 is 1.4 μm × 1.4 μm (centered). The implant resistor dimensions are 3.6 μm long and 6.0 μm wide. This cell was designed to extract the ohmic contact resistance dependence on the ohmic contact size and via 1 size. Figure 4.73 is a diagram of the contact geometry.
Array2.4×1.4_Nomet1 (EB4)

Array2.4×1.4_Nomet1 is a contact string with 304 gate metal-ohmic metal-S/D implant contacts and 304 metal 1-gate metal contacts with metal 1 and gate metal interconnect metals. The ohmic metal is 2.4 $\mu$m × 2.4 $\mu$m and the overlap with the gate metal “foot” is 1.4 $\mu$m × 1.9 $\mu$m. The metal 1 via to the gate metal is 1.4 $\mu$m × 1.4 $\mu$m. Metal 1 does not contact ohmic metal. The implant resistor dimensions are 3.6 $\mu$m long and 6.0 $\mu$m wide. This cell was designed to extract the ohmic contact resistance without metal 1 via. Figure 4.74 is a diagram of the contact geometry.
CHAPTER 4. E-O-E OEIC DEMONSTRATIONS

Ringosc (EB5)

Ringosc is a 23-stage ring oscillator with standard metal 1-ohmic metal contacts. Each inverter stage has a 10.0 \( \mu m \times 1.2 \mu m \) EFET with a 2.8 \( \mu m \times 3.4 \mu m \) DFET active load. Ohmic contact dimensions are the MESFET width \( \times 2.4 \mu m \) and the via 1 spacing is 0.5 \( \mu m \). Layout-extracted HSPICE inverter-delay is 110 ps. This cell was designed to extract the ring oscillator inverter delay with MESFET source and drain ohmic contacts having metal 1 interconnections.

Ringosc_Nomet1 (EB6)

Ringosc_Nomet1 is a 23-stage ring oscillator with standard gate metal-ohmic metal and standard metal 1-gate metal contacts. Each inverter stage has a 10.0 \( \mu m \times 1.2 \mu m \) EFET with a 2.8 \( \mu m \times 3.4 \mu m \) DFET active load. Metal 1 does not contact ohmic metal. Ohmic contact dimensions are the MESFET width \( \times 2.4 \mu m \) and the metal 1 via spacing is 0.5 \( \mu m \). Layout-extracted HSPICE inverter-delay is 88 ps. This cell was designed to extract the ring oscillator inverter delay with MESFET source and drain ohmic contacts having gate metal interconnections.

Inverter (EB7)

Inverter is a discrete inverter with a 10.0 \( \mu m \times 1.2 \mu m \) EFET and a 2.8 \( \mu m \times 3.4 \mu m \) DFET active load. Standard metal 1-ohmic metal contacts were used and ohmic contact dimensions are the MESFET width \( \times 2.4 \mu m \) and the metal 1 via spacing is 0.5 \( \mu m \). This cell was designed to extract the ring oscillator inverter I-V characteristics with MESFET source and drain ohmic contacts having metal 1 interconnections.

Inverter_Nomet (EB8)

Inverter_Nomet is a discrete inverter with a 10.0 \( \mu m \times 1.2 \mu m \) EFET and a 2.8 \( \mu m \times 3.4 \mu m \) DFET active load. Metal 1 does not contact ohmic metal. Standard gate metal-ohmic metal and standard metal 1-gate metal contacts. Ohmic contact
dimensions are the MESFET width $\times$ 2.4 $\mu$m and the metal 1 via spacing is 0.5 $\mu$m. This cell was designed to extract the ring oscillator inverter I-V characteristics with MESFET source and drain ohmic contacts having gate metal interconnections.

**Inverter_FETs (EB9)**

Inverter_FETs is composed of a discrete 10.0 $\mu$m $\times$ 1.2 $\mu$m EFET and a discrete 2.8 $\mu$m $\times$ 3.4 $\mu$m DFET. Standard metal 1-ohmic metal contacts were used and the ohmic contact dimensions are the MESFET width $\times$ 2.4 $\mu$m and the metal 1 via spacing is 0.5 $\mu$m. This cell was designed to extract the ring oscillator inverter FET I-V characteristics with MESFET source and drain ohmic contacts having metal 1 interconnections.

**Inverter_FETs_Nomet1 (EB10)**

Inverter_FETs_Nomet1 is composed of a discrete 10.0 $\mu$m $\times$ 1.2 $\mu$m EFET and a discrete 2.8 $\mu$m $\times$ 3.4 $\mu$m DFET. Standard gate metal-ohmic metal and standard metal 1-gate metal contacts were used and metal 1 does not contact ohmic metal. Ohmic contact dimensions are the MESFET width $\times$ 2.4 $\mu$m and the metal 1 via spacing is 0.5 $\mu$m. This cell was designed to extract the ring oscillator inverter FET I-V characteristics with MESFET source and drain ohmic contacts having gate metal interconnections.
4.8 Optical Bond Pad Chip (MIT-OEIC-4)

The final OEICs discussed in this chapter are on a chip that explores compact "optical bond pads," optical and electrical cross talk and digital optical logic. The chip is termed MIT-OEIC-4 and was designed in collaboration with J.F. Ahadian at MIT [126, 51]. The chip will be submitted in July, 1995, for fabrication at MOSIS/Vitesse (HGaAs3 four level metal process).

"Optical bond pads" (OBPs) are optical input and output devices with associated electrical drive and receive circuitry. These OBPs are functional optical interconnects with performance benefits previously discussed in Chapter 1. A portable collection of emitter and detector OBP "drop-in" cells can be included in a standard optoelectronic cell library, which is resident within a commercial circuit CAD package. The MIT-OEIC-4 OBPs were designed with Mentor Graphics GDT CAD software [136] but the OBPs can be exported for use with numerous other CAD packages. OBPs are intended to replace electrical signal bond pads and, therefore, should be competitive with electrical bond pads in size, power requirements and density. The OBPs on the MIT-OEIC-4 chip will be used to create OBP specification sheets for use with the OPTOCHIP project (see Section 5.4). Subsection 4.8.1 overviews the OBP OEICs.

Optical cross talk can arise from LEDs and external optical sources coupling into both the interlevel metal dielectric stack and the GaAs substrate. Electrical cross talk can arise from backgating effects (see Section 5.2 for a discussion of backgating in the Vitesse process) as well as capacitive and inductive coupling effects. These cross talk mechanisms limit the integration density and restrict the relative positioning of optical and electrical devices. A series of cells was designed, as overviewed in Subsection 4.8.2, to quantify cross talk mechanisms as well as to test solutions such as optical shields and backgate guard rings.

Optical interconnects and optoelectronic logic circuits, sometimes called "smart pixels," are the circuit and sub-system applications for the E-o-E optoelectronic integration technique. OBPs were designed to provide optical interconnect "drop in"
4.8. **OPTICAL BOND PAD CHIP (MIT-OEIC-4)**

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<tr>
<td>RTD RINGOSC</td>
<td>RTD-based ring oscillator.</td>
<td>326</td>
</tr>
</tbody>
</table>

Table 4.5: Section, page, physical name, cell name and description of all new OEICs on the MIT-OEIC-4 chip.

cells similar to bond pad “drop in” cells. OPBs can also be readily combined with DCFL logic and memory circuits to create functional digital optical logic circuits (e.g. AND, inverter and shift registers). Subsection 4.8.3 overviews a few canonical optical logic circuits.

Table 4.5 lists a brief summary of all new cells on the chip and should be used as an index. MIT-OEIC-3/NCIPT-OEVLISI-1 OEICs marked with a (*) symbol in Tables 4.3 and 4.4 will also be included on the MIT-OEIC-4 chip. Figure 4.75 shows the chip layout and Figure 4.76 shows the placement of most of the constituent OEIC cells.
Figure 4.75: MIT-OEIC-4 chip layout. Additional designs will be placed in the blank areas before fabrication.
Figure 4.76: MIT-OEIC-4 cell names. Additional designs will be placed the blank areas before fabrication.
4.8.1 OBP “Drop In” Cells

ARRAY LED A

ARRAY LED A is an eight element linear array of 50 μm × 50 μm LED DGWs with a center-to-center spacing of 100 μm. Each DGW is surrounded by an ohmic metal through metal 3 optical shield to reduce optical coupling into the dielectric stack. This array was designed to characterize LED uniformity and to serve as an optical source for matched detector arrays. Figure 4.77 is the schematic of the LED A circuit element and Figure 4.78 is the layout of the ARRAY LED A cell.

Figure 4.77: Schematic of the LED A circuit element.

Figure 4.78: Layout of the ARRAY LED A cell. Pads 2-9 are connected to the LED p-type terminals and pad 1 is connected to the LED n-type terminals.
ARRAY LED B

ARRAY LED B is an eight element linear array of DGWs identical to ARRAY LED A but with associated pull-down EFETs. A DCFL high signal applied to a drive EFET pulls the associated LED (active load) n-type terminal to the lower DCFL rail to turn the LED on. This array was designed to characterize LED and driver uniformity as well as to serve as an optical source for matched detector arrays.

Figure 4.79 is the schematic of the LED A circuit element and Figure 4.80 is the layout of the ARRAY LED B cell. Figure 4.81 is a plot of optical output power (Pout) vs. EFET L/W ratio for the LED circuit shown in the inset. A DCFL low input produces a Pout low below 1 nW and a DCFL high input produces a Pout high as shown. Three different efficiencies are plotted and the symbols represent ARRAY LED B EFET sizes, as summarized in Table 4.6.

![Figure 4.79: Schematic of LED B circuit element.](image)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>2</th>
<th>6</th>
<th>5</th>
<th>7</th>
<th>4</th>
<th>8</th>
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<tr>
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<td>1.2</td>
<td>3.0</td>
<td>5.0</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.6: ARRAY LED B device geometries referenced to gate pads.
Figure 4.80: Layout of ARRAY LED B cell. Pads 2-9 are connected to the EFET gates and pads 1 and 10 provide LED rail high and DCFL rail low biases.

Figure 4.81: Plot of optical output power (Pout) vs. EFET L/W ratio for the LED circuit shown in the inset. A DCFL low input produces a Pout low below 1 nW and a DCFL high input produces a Pout high as shown (assumes saturated EFET). Three different efficiencies are plotted and the symbols represent ARRAY LED B EFET sizes.
ARRAY OPFET A

ARRAY OPFET A is an eight element linear array of $40 \ \mu m \times 1.2 \ \mu m$ OPFET photodetectors, with $10 \ \mu m$ (source/drain)-to-gate spaces, and with a center-to-center spacing of $100 \ \mu m$. This array was designed to characterize OPFET uniformity and to serve as an optical detector for matched source arrays.

Figure 4.82 is the schematic of the OPFET A circuit element and Figure 4.83 is the layout of the ARRAY OPFET A cell.

![Figure 4.82: Schematic of OPFET A circuit element.](image)

![Figure 4.83: Layout of ARRAY OPFET A cell. Pads 2-9 are connected to OPFET drain terminals and pad 10 is connected to the OPFET source terminals.](image)
ARRAY OPFET B

ARRAY OPFET B is an eight element linear array of OPFETs identical to ARRAY OPFET A but with gate terminals. This array was designed to characterize tunable sensitivity OPFET uniformity (see Subsection 3.2.1) and to serve as an optical detector for matched source arrays.

Figure 4.84 is the schematic of the OPFET B circuit element. The layout of the ARRAY OPFET B cell is the same as the ARRAY OPFET A cell but with pad 1 connected to OPFET drain terminals and pads 2-9 connected to the OPFET gates.

![Schematic of OPFET B circuit element.](image)

Figure 4.84: Schematic of OPFET B circuit element.

ARRAY OPFET C

ARRAY OPFET C is an eight element linear array of OPFETs identical to ARRAY OPFET A but with associated DFETs. A high optical signal applied to the OPFET pulls the associated DFET (active load) source and output terminal to the lower DCFL rail. This array was designed to characterize OPFET receiver uniformity as well as to serve as an optical receiver for matched source arrays arrays.

Figure 4.85 is the schematic of the OPFET C circuit element and Figure 4.86 is the layout of the ARRAY OPFET C cell. Figure 4.87 is a plot of optical input power (Pin) vs. DFET gate length (L) for the OPFET C circuit shown in the inset. The
upper curve is the minimum Pin required to achieve a DCFL low (-1.9 V) output signal. The lower curve is the maximum allowable Pin to achieve a DCFL high (-1.4 V) output signal. The circles represent ARRAY OPFET C DFET sizes, as summarized in Table 4.7.

Figure 4.85: Schematic of OPFET C circuit element.

Figure 4.86: Layout of ARRAY OPFET C cell. Pads 2-9 are connected to output terminals and pads 1 and 10 provide DCFL high and low rail biases.

<table>
<thead>
<tr>
<th>Dimension</th>
<th>6</th>
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<th>3</th>
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<td>6</td>
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<td>12</td>
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</tbody>
</table>

Table 4.7: ARRAY OPFET C device geometries referenced to gate pads.
Figure 4.87: Plot of optical input power (Pin) vs. DFET gate length (L) for the OPFET C circuit shown in the inset. The upper curve is the minimum Pin required to achieve a DCFL low (-1.9 V) output signal. The lower curve is the maximum allowable Pin to achieve a DCFL high (-1.4 V) output signal. OPFETs were modeled as EFETs and optical input powers were converted to equivalent gate potentials using Equation 3.8.
ARRAY MSM A

ARRAY MSM A is an eight element linear array of 20 $\mu$m $\times$ 21 $\mu$m Schottky-diode gate metal MSM photodetectors with a center-to-center spacing of 100 $\mu$m. This array was designed to characterize MSM uniformity and to serve as an optical detector for matched source arrays.

Figure 4.88 is the schematic of the MSM A circuit element and Figure 4.89 is the layout of the ARRAY MSM A cell.

![Figure 4.88: Schematic of the MSM A circuit element.](image)

![Figure 4.89: Layout of the ARRAY MSM A cell. Pads 2-9 are connected to MSM “drain” terminals and pad 10 is connected to MSM “source” terminals.](image)
ARRAY MSM B

ARRAY MSM B is an eight element linear array of MSMs identical to ARRAY MSM A but with associated transimpedance amplifiers [75]. A high optical signal applied to the MSM produces a DCFL high signal at the amplifier output. This array was designed to characterize MSM receiver uniformity as well as to serve as an optical receiver for matched source arrays.

Figure 4.90 is the schematic of the MSM B circuit element and Figure 4.91 is the layout of the ARRAY MSM B cell. Figure 4.92 is a plot of the transimpedance amplifier output voltage as a function of the input current for three different DFET feedback resistor gate biases (-0.45 V, -0.50 V and -0.55 V). Typical MSM responsivities of \(~0.3\) A/W allow input currents to be converted to equivalent optical input powers.

![Schematic of MSM B circuit element](image)

**Figure 4.90**: Schematic of MSM B circuit element.
Figure 4.91: Layout of ARRAY MSM B cell. Pads 2-5 and 6 provide DFET gate biases, pads 7-10 and 12-15 are connected to the amplifier outputs and pads 1 and 11 provide DCFL rail biases.

Figure 4.92: Plot of the transimpedance amplifier output voltage as a function of the input current for three different DFET feedback resistor gate biases (-0.45 V, -0.50 V and -0.55 V for the upper, middle and lower curves as low currents, respectively) [143]. Typical MSM responsivities of ~0.3 A/W allow input currents to be converted to equivalent optical input powers.
4.8.2 Cross talk related cells

CROSSTALK A

CROSSTALK A consists of an LED DGW with four surrounding OPFETs. The DGW measures 50 \( \mu \text{m} \times 50 \ \mu \text{m} \) and the OPFETs measure 40 \( \mu \text{m} \times 20 \ \mu \text{m} \) with 10 \( \mu \text{m} \) (source/drain)-to-gate spacing. The inner edges of all OPFETs are 10 \( \mu \text{m} \) from the DGW sidewall. Two backgate taps are included at distances of 15 \( \mu \text{m} \) and 35 \( \mu \text{m} \) from two OPFETs. This cell was designed to determine if LED optical emission is coupled into the inter-level dielectric stack or into the substrate, an effect which is important for understanding optical cross talk. OPFETs monitor optical intensities and directional uniformity. Backgate taps allow the effects of LED bias induced OPFET backgating to be factored from the OPFET signals.

Figure 4.8.2 shows the layout of the CROSSTALK A cell.

Figure 4.93: Layout of CROSSTALK A cell. Pads 2-3, 5-6, 8-9 and 11-12 are connected to the OPFET drain and source terminals. Pads 1 and 10 are connected to backgate taps and pads 4 and 6 supply the LED bias.
CROSSTALK B

CROSSTALK B is identical to CROSSTALK A except that the inner edges of the OPFETS are 10 μm, 20 μm, 30 μm and 50 μm from the DGW sidewall. This cell was designed to determine the attenuation of side emitted optical power which is important for understanding optical cross talk. CROSSTALK A measurements allow directional optical emission nonuniformity to be factored from the OPFET signals.

Figure 4.94 shows the layout of the CROSSTALK B cell.

![Figure 4.94: Layout of CROSSTALK B cell. Pads 2-3, 5-6, 8-9 and 11-12 are connected to the OPFET drain and source terminals. Pads 1 and 10 are connected to backgate taps and pads 4 and 6 supply the LED bias.](image-url)
CROSSTALK C

CROSSTALK C is identical to CROSSTALK A except that the inner edges of the OPFETS are 20 μm from the DGW sidewall and an optical shield surrounds the LED DGW. The shield is 6.0 μm wide and was formed by stacking the following layers: ohmic metal, via 1, metal 1, via 2, metal 2, via 3 and metal 3. This cell was designed to characterize how well the optical shield blocks side emitted light. A bias can be applied to the shield to serve as a backgate guard ring while backgate taps allow the effects of LED bias induced OPFET backgating to be factored from the OPFET signals.

Figure 4.95 shows the layout of the CROSSTALK C cell.

Figure 4.95: Layout of CROSSTALK C cell. Pads 2-3, 5-6, 8-9 and 11-12 are connected to the OPFET drain and source terminals. Pads 1 and 10 are connected to the shield (with S/D implanted tap) and backgate tap, respectively. Pads 4 and 6 supply the LED bias.
CROSSTALK D

CROSSTALK D is identical to CROSSTALK C except that the optical shield was formed by stacking the following layers: metal 1, via 2, metal 2, via 3 and metal 3. This cell was designed to characterize how well the metal 1 - metal 3 optical shield blocks side emitted light and, therefore, if the side emitted light is guided in the upper levels of the dielectric stack.

Figure 4.96 shows the layout of the CROSSTALK D cell.

![CROSSTALK D Diagram]

Figure 4.96: Layout of CROSSTALK D cell. Pads 2-3, 5-6, 8-9 and 11-12 are connected to the OPFET drain and source terminals. Pads 1 and 10 are connected to backgate taps and pads 4 and 6 supply the LED bias.
CROSSTALK E

CROSSTALK E is identical to CROSSTALK C except that the optical shield was formed by stacking the following layers: ohmic metal, via 1 and metal 1. This cell was designed to characterize how well the ohmic metal - metal 1 optical shield blocks side emitted light and, therefore, if the side emitted light is guided in the lower levels of the dielectric stack.

Figure 4.97 shows the layout of the CROSSTALK E cell.

Figure 4.97: Layout of CROSSTALK E cell. Pads 2-3, 5-6, 8-9 and 11-12 are connected to the OPFET drain and source terminals. Pads 1 and 10 are connected to the shield (with S/D implanted tap) and backgate tap, respectively. Pads 4 and 6 supply the LED bias.
CROSSTALK F

CROSSTALK F consists of two OPFET detectors (sized as in previous cells), one with a backgate guard ring, and various backgate taps. One OPFET has a S/D implanted guard ring with ohmic metal and metal 1 to allow external biases to be applied. The OPFET with the guard ring has four backgate taps: two 10 μm and two 15 μm from the edge of the OPFET. The other OPFET has three backgate taps: two 10 μm and one 15 μm from the OPFET edge. This cell was designed to characterize the electrical cross talk between two detectors. An optical signal applied to one OPFET will increase the backgate potential leading to increased dark current on the other OPFET. The guard ring and backgate taps allow this cross talk to be characterized. The guard ring operating voltage necessary to minimize photo-induced backgate cross talk can also be determined.

Figure 4.98 shows the layout of the CROSSTALK F cell.

Figure 4.98: Layout of CROSSTALK F cell. Pads 2-3 and 8-9 are connected to the OPFET sources and drains, pads 1, 5, 7 and 11 to the 10 μm spaced taps and pads 6, 10 and 12 to the 15 μm spaced taps. Pad 4 contacts the guard ring.
CROSSTALK G

CROSSTALK G consists of four OPFET detectors (sized as in previous cells), three shielded from the fourth by an optical shield and a metal 3 “roof”, and various backgate taps. One of the three shielded OPFETs also has a backgate guard ring. This cell was designed to determine the photo-induced backgate cross talk between OPFETs, as does CROSSTALK F, except that stray optical signals are shielded. This allows the backgate effect to be isolated from stray optical probe signals. The OPFET with the guard ring can be used to determine the guard ring operating voltage necessary to minimize the photo-induced backgate cross talk.

Figure 4.99 shows the layout of the CROSSTALK G cell.

Figure 4.99: Layout of CROSSTALK G cell. Pads 2-3, 8-9 and 11-12 are connected to the shielded OPFET sources and drains. Pads 5-6 are connected to the unshielded OPFET source and drain. Pads 7, 10 and 12 are connected to backgate taps.
4.8.3 Optical logic related cells

OIO INV

OIO INV is an optical input to optical output logical inverter circuit. OIO INV consists of an OPFET C (with 6 μm × 16 μm DFET) inverting detector circuit driving an LED B (with 100 μm × 1.2 μm EFET) noninverting circuit which produces an optical output signal. All detector and emitter center-to-center spacings are 100 μm. This cell was designed to demonstrate a digital optical inverter circuit, which is important for optical logic systems, built from “drop in” OBP circuits.

Figure 4.100 shows the layout of the OIO INV cell.

![Diagram](image1)

Figure 4.100: Layout of the OIO INV cell. Pad 1 supplies the LED p-type terminal bias and pads 2 and 3 provide the DCFL rail biases.

OIO AND

OIO AND is an optical input to optical output logical AND circuit (also a logical NOR circuit with inverted inputs). OIO AND consists of two OPFET C (with 6 μm × 16 μm DFET) inverting detector circuits driving a two input NOR circuit (MIT-OEIC-3 SEED NOR circuit). The NOR output drives an LED B (with 100 μm × 1.2 μm EFET) noninverting circuit which produces an optical output signal. All detector and emitter center-to-center spacings are 100 μm. This cell was designed to demonstrate a digital optical AND circuit, which is important for optical logic
systems, built from “drop in” OBP circuits.

Figure 4.101 shows the layout of the OIO AND cell.

Figure 4.101: Layout of OIO AND cell. Pad 1 supplies the LED p-type terminal bias and pads 2 and 3 provide the DCFL rail biases.

Figure 4.102: Layout of the OIO D FLIP FLOP cell. Pad 1 supplies the LED p-type terminal bias and pads 2 and 3 provide the DCFL rail biases.

Figure 4.103: Layout of the OIO PROBE cell. Pads 1-2 and 6-7 are connected to the LED DCFL inputs and OPFET DCFL output, respectively. Pad 4 supplies the LED p-type terminal bias and pads 3 and 5 provide the DCFL rail biases.
4.8. **OPTICAL BOND PAD CHIP (MIT-OEIC-4)**

**OIO D FLIP FLOP**

OIO D FLIP FLOP is an optical input (data and clock) D-type flip flop with optical outputs (Q and \( \bar{Q} \)). OIO D FLIP FLOP consists of two OPFET C (with 6 \( \mu m \times 16 \mu m \) DFET) inverting detector circuits driving the data and clock inputs of a D flip flop circuit (MIT-OEIC-3 D FLIP FLOP circuit). The D flip flop Q and \( \bar{Q} \) outputs drive LED B (with 100 \( \mu m \times 1.2 \mu m \) EFET) noninverting circuits which produces an optical output signals. The two OPFETs are separated, and thereby optically shielded, with an optical shield (ohmic metal - metal 4) and the D flip flop circuit is shielded from stray surface-normal optical signals with a metal 3 “roof”. All detector and emitter center-to-center spacings are 100 \( \mu m \). This cell was designed to demonstrate a digital optical memory circuit, which is important for optical logic systems, built from “drop in” OBP circuits.

Figure 4.102 shows the layout of the OIO D FLIP FLOP cell.

**OIO PROBE**

OIO PROBE is an optical input and optical output circuit for use in testing (probing) all circuits with detector and emitter center-to-center spacings of 100 \( \mu m \). OIO PROBE consists of two OPFET C (with 6 \( \mu m \times 16 \mu m \) DFET) inverting detector circuits and two LED B (with 100 \( \mu m \times 1.2 \mu m \) EFET) noninverting circuits. This cell was designed to serve as a convenient detector and emitter pitch-matched circuit for testing various optoelectronic circuits. A chip with the OIO PROBE circuit can be positioned face-to-face with a chip containing the OEIC to be tested.

Figure 4.103 shows the layout of the OIO PROBE cell.
RTD RINGOSC

RTD RINGOSC is a 23 stage ring oscillator with EFETs, DGWs for epitaxially grown RTDs and a DCFL output stage. This cell was designed by R.J. Aggarwal at MIT [63, 141] and layed out as part of the MIT-OEIC-4 chip. Each stage of the RTD RINGOSC circuit consists of an EFET (40 $\mu$m $\times$ 1.2 $\mu$m) pull-down transistor and a DGW region for an epitaxially grown RTD active load. A two-stage DCFL buffer (40 $\mu$m $\times$ 1.2 $\mu$m EFET with a 10 $\mu$m $\times$ 3.0 $\mu$m DFET inverter and an 84 $\mu$m $\times$ 1.2 $\mu$m EFET with a 20 $\mu$m $\times$ 3.0 $\mu$m DFET inverter) serve as an output pad driver. This cell was designed to characterize the power-speed product of RTD based inverter stages, which are potentially useful for high-speed and low-power logic and SRAM circuits.

Figure 4.104 shows the layout of the RTD RINGOSC cell.

![Image of RTD RINGOSC cell layout]

Figure 4.104: Layout of the RTD RINGOSC cell. Pads 1 and 2 provide ring oscillator ground and power, pads 4 and 5 provide DCFL high and low rail biases and pad 3 is the ring oscillator output.
Chapter 5

Conclusions and Continuing Research

Optical interconnects (OIs) offer solutions to several inherent electrical interconnect performance limitations. Reduced cross talk, lower drive powers, higher bandwidths and optional transmission media enable OIs to achieve superior performance with both existing and new interconnect architectures (Section 1.1). OIs consist of optical emitters or modulators, optical detectors and associated electronic circuitry. Large-scale high-density OI systems require the monolithic integration of optical and electrical devices, forming optoelectronic integrated circuits (OEICs). At present, OI systems are limited by the inability to fabricate VLSI-level OEICs (Section 1.2). A novel optoelectronic integration technique capable of producing VLSI OEICs was proposed, developed and demonstrated in this work.

The Epitaxy-on-Electronics (E-o-E) optoelectronic integration technique involves epitaxial growth of optical device heterostructures on fully processed VLSI GaAs MESFET electronic circuits (Section 2.1). A commercially available, refractory-metal enhancement- and depletion-mode MESFET process was shown to be stable after 5 hour, 470°C molecular beam epitaxy (MBE) growths with intrinsic devices surviving beyond 5 hours at 525°C (Section 3.1). Based on this thermal stability, circuits were
designed and commercially fabricated to serve as the OEIC electronics (Section 2.3). The electronic circuits GaAs substrate also serves as the optical device substrate. During circuit design, openings through the interlevel dielectric stack to the GaAs substrate, termed dielectric growth wells (DGWs), were also specified by stacking two standard process etch layers (Section 2.2). Optical device heterostructures were grown on the chips by MBE at lowered growth temperatures, resulting in epitaxial material in the DGWs (epi-islands) (Sections 2.4 and 2.5). The polycrystalline material in the inter-DGW regions was removed yielding a quasi-planar surface. Optical devices were processed in the epi-islands using conventional fabrication processes (Section 2.6). Source/drain n-type ion-implants with standard ohmic contacts at the bottom of the DGWs and top-side p-type ohmic metal provided terminal access to the optical devices. The OEICs were completed by metallizing the top optical device contact to upper level metal pads connected to the electronics (Section 2.6). Fully functional OEICs were optically and electrically characterized (Section 2.7).

In conjunction with collaborators, numerous optical devices were demonstrated to be compatible with E-o-E fabrication. High-speed metal-semiconductor-metal (MSM) and high-gain optical-enhancement FET (OPFET) detectors were designed, fabricated in the commercial MESFET process and characterized (Section 3.2). (In,Al,Ga)As LEDs, in-plane laser diodes, in-plane surface-emitting laser (IPSEL) diodes and multiple quantum well modulators/detectors were designed, MBE grown at E-o-E compatible temperatures, processed and characterized (Sections 3.3 and 3.4). (In,Ga)AsP LEDs and laser diodes were evaluated and determined to be optimal for E-o-E integration (Section 3.3).

Nine E-o-E based OEIC chips were designed, fabricated and characterized in association with several collaborators. Among the OEICs demonstrated with these chips were analog neural-inspired threshold circuits with LEDs and OPFETs (Section 4.1), analog neural-inspired winner-take-all circuits with LEDs and OPFETs (Sections 4.2-4.5), and digital transmit/receive high-speed circuits with MSMs, LEDs and IPSELs
(Section 4.6). A multi-epitaxy chip, with over fifty OEICs to develop five different optical devices (Section 4.7), and an “optical bond pad” chip, to develop drop-in cells for optical interconnects (Section 4.8), were also designed.

While E-o-E based OEICs are routinely fabricated, several design, growth and process refinements are anticipated. The remainder of this chapter suggests future research and development directions. These suggestion sections also review the current E-o-E technology status and, thereby, serve as additional conclusions. Section 5.1 discusses DGW design and the dielectric stack in the context of improved epitaxial material quality and process uniformity. The backgating effect, its consequences and three preliminary solutions are presented in Section 5.2. Section 5.3 reviews the current status and condition of post-E-o-E integration bond pads which are important for final OEIC packaging. Finally, to provide the E-o-E technology to a wider user community, a multiproject chip termed OPTGCHIP, whereby several research groups jointly fabricate E-o-E based OEICs, is scheduled and represents the evolution of this work (Section 5.4).

5.1 DGWs and the Dielectric Stack

E-o-E epitaxial growth quality and device fabrication flexibility can be improved by investigating and possibly modifying the dielectric growth well and dielectric stack design. DGWs can be designed with or without S/D ion implants, with nominally vertical or angled sidewalls and in a variety of sizes (geometries). The dielectric stack planarity and total thickness determines the possible lithography techniques and the required epitaxial thickness, respectively. This section briefly discusses the tradeoffs involved with DGW and dielectric stack design and modifications.

DGWs with S/D n+ ion implants and standard ohmic metal contacts are advantageous because only one top-side ohmic contact, and one mini-pad to connect back to the circuit, is required. The integration density is, therefore, higher than if two top-
side contacts are required. The fabrication flow also requires one less metallization step. The possible disadvantage of ion-implanted DGWs is that the DGW substrate crystalline quality may be reduced by the \( n^+ \) implant. The S/D implant is annealed at 800°C for one hour and most of the implant energy induced damage is nominally removed. 1000× Nomarski optical microscopy does not reveal any morphology in the S/D implanted DGWs. LED heterostructures, a total of ~4.2 \( \mu \)m thick and grown with AlGaAs/GaAs or InGaAs/GaAs superlattices to impede defect propagation, were grown in S/D implanted DGWs. The LED top-surface epitaxy does not have any morphology (1000× Nomarski optical microscopy and scanning electron microscopy (SEM)) and the epitaxial layers appear flat and smooth (SEM). Quantum wells in similarly grown epitaxial layers have strong photoluminescence peaks and functional LEDs have been demonstrated.

To further investigate the quality of epitaxy grown in S/D implanted DGWs, a chip with four \( \text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs} \) quantum wells (same sample as presented in Figure 4.40) has been sent to one of our sponsors/collaborators, J. Fitz at Ft. Meade, for x-ray topography and two-dimensional scanning cathodoluminescence analysis. Two-dimensional scanning cathodoluminescence analysis is also being performed by R.J. Aggarwal [63] in collaboration with Prof. Fitzgerald's group at MIT.

The Well Array cell on the MIT-OEIC-3 chip contains several series of DGWs with full S/D implant, with partial S/D implant and without S/D implant. A comparative, quantitative side-by-side study of material quality can be conducted with this array. The partial S/D implanted DGWs have roughly 25% of the total DGW area implanted. This area is rectangular and is adjacent to the ohmic contact. The concept of a partially implanted DGW is that a small implanted region can contact the first grown \( n^+ \) epitaxial layers and the total n-terminal access resistance is not compromised. Epitaxial devices would then be grown on primarily nonimplanted, possibly higher quality, DGW substrate regions but still have a standard ohmic metal n-type conduction path. Visual inspection and surface profilometer (Dektak) traces
on the partially S/D implanted DGWs revealed that the implanted regions are depressed by ~150 Å compared to the non-implanted areas [51, 63]. This difference is possibly due to ion-implantation sputtering [51]. The implanted area morphology appears identical (1000× Nomarski optical microscopy) to the nonimplanted area. The effects of this ~60 monolayer step on subsequent material and device quality require further investigation.

DGW size, and possibly sidewall profile for small DGWs, can also influence epitaxial material quality. The Well Array cell on the MIT-OEIC-3 chip contains several series of square DGWs with side lengths ranging from 100 μm to 5 μm. Vertical and angled DGW sidewalls are also included in this cell. The vertical sidewalls were designed by identically sizing and aligning the passivation and scribe-lane etch layers. Angled sidewalls, which always slope outward from bottom to top, can be fabricated by designing the scribe-lane etch to be larger than the passivation etch. The scribe-lane etch layer extends past the passivation etch layer by 2.0 μm for the angled DGWs in the Well Array cell. Nearly arbitrary sidewall angles can be fabricated by stacking via etches (design rule violation) with various offsets and possibly interlevel metal etch stops to prevent over-etching (see LED Mirror cell in Subsection 4.7.3). An SEM and two-dimensional scanning cathodoluminescence analysis of these DGWs should reveal the material quality dependence on DGW size and sidewall profile.

In addition to high-quality epitaxial material, advanced heterostructure devices require high-resolution lithography. Contact lithography requires physical contact between the mask plate and the photoresist-covered semiconductor crystal. As the distance between the mask plate and the photoresist increases, mask alignment becomes more difficult and diffraction effects broaden patterned linewidths. Projection lithography, which projects and focuses UV light through a mask, does not require physical contact with the photoresist. Contact lithography is particularly sensitive to nonplanarity in photoresist surface. Photoresist edge buildups, typically several microns thick, must be removed from the sample to achieve good alignment and
Figure 5.1: Schematic cross section of a bond pad (left), DGW (middle), DGW sidewalls (middle left and right) and dielectric/metal stack (right) for the Vitesse HGaAs3 process with (a) three metal levels and (b) four metal levels. See Section 2.3, Table 2.1 for detailed dimensions [28, 31].
5.1. **DGWS AND THE DIELECTRIC STACK**

Linewidths. E-o-E lithography on fully processed chips suffers from nonplanar dielectric stack top surfaces (discussed below). While projection lithography is insensitive to nonplanar dielectric stack surfaces, and is the optimal lithography system for E-o-E based OEICs, projection lithography aligners are not abundant in research labs (1.0-μm-wide openings were patterned at MIT Lincoln Labs using a 4:1 Canon projection aligner [91, 140]). Contact lithography aligners will be used in the immediate future and for this reason possible design modifications are suggested.

Figure 5.1 shows a schematic cross section of a bond pad (left), DGW (middle), DGW sidewalls (middle left and right) and dielectric/metal stack (right) for the Vitesse HGaAs3 process with (a) three metal levels and (b) four metal levels. See Section 2.3, Table 2.1 for detailed dimensions [28, 31]. Figure 5.1 is drawn to scale (vertically) but the right-angle surface features represent the design dimensions, not the realistic step coverage and surface smoothing. The HGaAs3 three-metal process (without metal 4 and referred to as process (a)), which was available from Vitesse until 1993 and had a dielectric stack nearly identical to the HGaAs2 process), had a maximum dielectric stack height of 8.8 μm. This is 3.9 μm thinner than the maximum dielectric stack height of the current four-level metal HGaAs3 process (12.7 μm), which is referred to as process (b). DGWs are typically formed with dielectric layer sidewalls (i.e. interlevel metal ≥ ~20 μm from the DGW sidewall) which had a total thickness of 4.4 μm for process (a) but a total thickness of 5.8 μm for process (b). A final observation before discussing the consequences of these dimensions is that the bond pad perimeters also have tall features. Bond pads in process (a) extended a total of 3.4 μm above the DGW sidewall while process (b) bond pads (as currently designed) extend 5.3 μm above the DGW sidewall [63, 52].

The difference between the maximum dielectric stack height and the dielectric sidewall height (4.4 μm and 6.9 μm for process (a) and (b), respectively) is the minimum distance between the contact mask plate and the top epitaxial surface (nominally aligned with the top of the dielectric sidewall). Current Vitesse design
rules specify that all interlevel metal levels (metal 1 - metal 4) can be stacked and that metal 4 should only be used for large ground planes and bond pads [28]. This implies that the 12.7 μm maximum dielectric stack height can occur in random locations across a chip. To help level a contact mask, several maximum height dielectric stack "pillars" or rows could be placed across the chip, thereby providing a level surface on which the mask can rest. While this will help increase lithography uniformity, it still results in a large mask-photoresist distance (6.9 μm). This distance can be reduced by restricting the use of metal 4 to only bond pads, where a via 4 etch (1.5 μm) and the absence of metal 1 (1.05 μm) and metal 2 (1.45 μm) (see below) would reduce the maximum dielectric stack height to ~8.7 μm, except for around the edge of the bond pad (discussed below). With this design restriction the mask-photoresist distance would be reduced from 6.9 μm to 2.9 μm, which is less than the 4.4 μm mask-photoresist distance on the MIT-OEIC-1 chip (HGAs3 with three-level metal process (a)) which had 3.5 μm openings and 4.0 μm lines successfully patterned using contact lithography as part of the IPSEL integration.

Another design modification which can reduce the mask-photoresist (mask-top epitaxial surface) distance is to increase the DGW sidewall height and to continue to align the top epitaxial surface with the top DGW sidewall surface. By designing interlevel metal layers in the DGW sidewall stack the sidewall stack height can be increased all the way up to the maximum dielectric stack height (i.e. 12.7 μm). The metal layers must be recessed from the DGW sidewall by ~5 μm, and therefore encapsulated in electrically insulating dielectric, to avoid shorting with the epitaxial layers. The advantage of increasing the DGW sidewall height is that a nearly planar top surface can be achieved. The drawback is that the total growth thickness, and therefore growth time, is significantly increased (growth time is linearly proportional to growth thickness). The E-o-E thermal budget (5 hours at or below 470°C) must not be exceeded. It is possible to grow conducting epitaxial material at a temperature low enough (e.g. 400º) to allow nearly twelve-hour growths (1 μm/hour is a typical
5.1. DGWS AND THE DIELECTRIC STACK

MBE growth rate). Most growths in this work were 4.2 μm thick and were designed to match the DGW sidewall thickness on MIT-OEIC-1 chips (process (a)).

The final dielectric stack design modification to reduce the mask-photoresist distance, as well as increase planarity for improved photoresist spin uniformity, regards bond pad design. As shown in Figure 5.1 (b), most of the bond pad is nearly level with the top of the DGW sidewall (~1 μm above). The bond pad "lip", however, extends several additional microns because the standard Vitesse design rules require vias to be inside underlying metal layers by ~3.5 μm. The oxide layers contribute to the overall "lip" height. Bond pads which violate this design rule could be designed such that no oxide layers are at the edge of the bond pad (except for the passivation layer which must extend across the bond pad edge to hold the pad in place). Identically sizing and aligning the via layer and underlying metal layer is one possible solution. Bond pad designs should be fabricated to verify this approach, specifically to quantify misalignment tolerances, since a via layer offset with respect to, or larger than, the underlying metal layer would result in a deep etched trench around the underlying metal (i.e. no metal etch stop at perimeter). A via layer larger than the underlying metal has the advantage of having a known edge profile (i.e. a deep trench around the perimeter) because the pad perimeter topology is insensitive to alignment tolerances. Another design modification, which should be performed, is to not include the metal 2 layer in the pad. Metal 2 was included both as a carry over from HGaAs3 three level metal designs as well as to produce thick, supple bond pads for improved post-growth probing.

A variety of improved DGW and dielectric stack design test cells are included on the MIT-OEIC-4 chip [126]. Various metal-dielectric layer stack combinations are also included to measure realistic cross-sectional dimensions which are important for understanding photoresist spin profiles and ultimate lithography uniformity.
5.2 Backgating Effect

In addition to the gate metal "front-side" MESFET gate, there is a "back-side" MESFET gate which also affects the transistor source-drain current. This "back-side" gate is termed a backgate. The backgate in the Vitesse process is formed when the semi-insulating LEC grown GaAs wafers are lightly p-type ion implanted to a depth of approximately 1 μm. The p⁻ ion implanted layer increases MESFET threshold voltage uniformity because the uniform doping of the nonuniform mid-band gap traps inherent in the semi-insulating substrate (the p⁻ concentration is greater than the trap concentration). However, the consequence is that a conducting sheet beneath and between MESFETs is formed. This p⁻ layer forms a p⁻n junction with the MESFET channel and the potential across this junction determines the total depletion width. A reverse biased p⁻n junction will extend the n-side depletion region into the channel and thereby reduce the channel current. The influence of the p⁻ layer potential on the channel current is termed the backgating effect. Our collaborator A.C. Grot at Caltech [69, 70], in communication with MIT [123], has examined the impact of the backgating effect on E-o-E based OEIC devices and has proposed possible solutions. This review of A.C. Grot's work serves as background for the backgate-reduction circuits presented in Chapter 4 and for future research.

The p⁻ backgate layer is not explicitly contacted in the Vitesse process (i.e. there is not a p⁺ ohmic contact in the standard process). Near S/D n⁺ contacts, however, the backgate potential does not exceed the S/D contact potential. This is because a backgate potential greater than the S/D contact would result in a forward biased p⁻n⁺ junction resulting in current flow which is not possible because there is no ohmic contact to the p⁻ layer (i.e. the backgate is floating). The backgate potential can be lower than the S/D potential because this reverse biases the p⁻n⁺ junction (e.g. a positive S/D bias does not result in positive backgate potential). The backgate potential distribution is, therefore, a complicated function of the local S/D contact potentials and distribution. In the limit of very dense S/D contacts, typical of digital
5.2. **BACKGATING EFFECT**

VLSI DCFL circuits, the S/D n⁺ contacts sufficiently deplete the backgate layer such that backgating is not a concern [53, 69]. Backgating is also not a problem in the high-speed operation limit since beyond ~10-100 kHz the high resistivity and low current backgate does not follow the S/D potentials [70]. Backgating is a concern, however, for high-voltage circuits, which have large S/D potential differences, for OFETs, which rely on photomodulated backgate potentials for high gain, and for DCFL circuits which may not be highdensity or highspeed. A simple backgating model is required to show why the backgating effect is important for certain E-o-E based OEICs.

Backgating can be modeled, after linearizing the depletion-width term, as a correction term to the threshold voltage [146] as follows:

\[ V_T = V_{TO} + K_{bg}(V_S - V_{SS}) \]  \hspace{1cm} (5.1)

\( V_T \) is the effective threshold voltage, \( V_{TO} \) is the threshold voltage without backgate effects, \( K_{bg} \) is the backgating coefficient, \( V_S \) is the MESFET source (lower potential than drain) and \( V_{SS} \) is the backgate potential. \( K_{bg} \) has been experimentally determined to be ~0.08 for the Vitesse HGaAs2 process [70, 146]. Equation 5.1 indicates that the backgating effect depends on the difference between the backgate potential and the source potential. With this simple model the effect of backgating on EFETs, DFETs and OFETs can be understood.

Figure 5.2 shows EFET I-V characteristics (\( V_S \) held at 0.0 V) with a fixed gate-source voltage (\( V_{GS} = 0.34 \) V) for backgate potentials swept from 0.0 V to -1.0 V. The backgate potential was applied through a proximal S/D contact. The drain-source current dropped by nearly 80% for \( V_{SS} = -1.0 \) V while positive S/D potentials had no effect (i.e. identical to the 0.0 V curve). EFETs are especially susceptible to backgating effects because of the relatively low channel doping concentration. In standard DCFL circuits, however, EFET backgating effects are minimal. This is because DCFL circuits typically have EFET sources connected to the lower DCFL
Figure 5.2: EFET I-V characteristics ($V_S$ held at 0.0 V) with a fixed gate-source voltage ($V_{GS} = 0.34$ V) for backgate potentials swept from 0.0 V to -1.0 V [70].

rail (-2.0 V for 0.0 V and -2.0 V DCFL rails) which is usually the lowest potential in the circuit (i.e. $V_{SS}$). Unless a S/D contact, which is sometimes referred to as a backgate tap, with a bias less than -2.0 V appears on the chip the EFET does not experience backgating effects. Backgate diagnostic circuits in Subsections 4.7.1 and 4.8.2 were designed to determine the distance at which a backgate tap, with bias less than -2.0 V, affects EFET performance.

Figure 5.3 shows a DFET normalized drain-source current vs. backgate voltage for gate voltages swept from 0.0 V to -0.8 V. $V_S$ was held at 0.0 V, $V_{DS}$ was maintained at 1.0 V and the drain-source current was normalized to the drain-source current flowing at 0.0 V backgate potential for the particular $V_G$. A significant reduction in channel current occurs for backgate voltages below -0.5 V, due to the backgate effect, for DFETs operated near or below threshold. Above threshold, however, the backgate effect is reduced due to the increased carrier concentration in the channel. Digital DCFL circuits typically use resistor-connected ($V_{GS} = 0.0$ V) DFETs as active loads for inverters. Figure 5.3 indicates that resistor-connected DFETs are less sensitive to backgating effects, though the channel current is reduced which will increase inverter
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Figure 5.3: DFET normalized drain-source current vs. backgate voltage for gate voltages swept from 0.0 V to -0.8 V. $V_S$ was held at 0.0 V, $V_{DS}$ was maintained at 1.0 V and the drain-source current was normalized to the drain-source current flowing at 0.0 V backgate potential for the particular $V_G$ [70].

Figure 5.4: Post-growth (5 hours at 530°C) DFET normalized drain-source current vs. backgate voltage for gate voltages swept from 0.0 V to -0.8 V. $V_S$ was held at 0.0 V, $V_{DS}$ was maintained at 1.0 V and the drain-source current was normalized to the drain-source current flowing at 0.0 V backgate potential for the particular $V_G$ [70].
Figure 5.5: OPFET drain-source current ($V_S = 0.0$ V, $V_{DS} = 1.0$ V) vs. backgate potential for optical input powers swept from 0.0 nW to 100 nW [70].

delay times. Non-resistor-connected DFETs are, however, susceptible to backgating effects.

Figure 5.4 shows a post-growth (5 hours at 530°C) DFET normalized drain-source current vs. backgate voltage for gate voltages swept from 0.0 V to -0.8 V. $V_S$ was held at 0.0 V, $V_{DS}$ was maintained at 1.0 V and the drain-source current was normalized to the drain-source current flowing at 0.0 V backgate potential for the particular $V_G$. Compared with Figure 5.3, Figure 5.4 shows that the backgating effect sensitivity has decreased substantially after epitaxial growth (e.g. thermal cycling). Apparently the backgate layer p− concentration has been reduced, though a physical mechanism has not been identified. These data are complicated by the fact that the S/D contact ohmic contact resistance increased substantially during the growth and the total indicated $V_g$ biases are not reaching the backgate. Figure 5.5 shows an OPFET drain-source current ($V_S = 0.0$ V, $V_{DS} = 1.0$ V) vs. backgate potential for optical input powers swept from 0.0 nW to 100 nW. At low optical input powers backgating is a significant effect. As optical input powers increase and approach 100 nW the OPFET backgate sensitivity decreases. It is expected that OPFETs are sensitive to
5.2. BACKGATING EFFECT

Figure 5.6: OPFET drain-source current ($V_{GS} = 0.0$ V, $V_{DS} = 0.3$ V) as a function of optical input power for Gen. 2 and Gen. 3 chips (N2CM and N35U Vitesse runs, respectively) both with and without negative backgate biases [70].

backgating effects since the OPFET operating principle is the backgate mechanism (see Subsection 3.2.1). If an OEICs optical operating powers are on the order of 100 nW backgating is not a significant concern. If, however, typical operating powers are designed to be on the order of 10 nW or lower, backgate effects need to be minimized. OPFET-based receiver cells should be designed with the OPFET source connected to the lower DCFL rail to minimize backgating effects (see Subsection 4.8.1). It is also important to note that OPFET dark current increases for positive backgate potentials (not accurately reflected in Figure 5.5 because the backgate potential was applied to a S/D n+ contact and not directly to the backgate). If two OPFETs are positioned close to each other and an optical signal is applied to one OPFET the dark current of the other OPFET will increase. This is because the backgate potential is increased (see Subsection 3.2.1 for photovoltage expression) which decreases the channel depletion width on the dark OPFET, thereby allowing increased drain-source current to flow. The optical and electrical crosstalk circuits presented in Subsection 4.8.2 were designed to quantify the minimum separation between OPFETs.
CHAPTER 5. CONCLUSIONS AND CONTINUING RESEARCH

Figure 5.6 shows OPFET drain-source currents \((V_{GS} = 0.0 \text{ V}, V_{DS} = 0.3 \text{ V})\) as a function of optical input power for Gen. 2 and Gen. 3 chips (N2CM and N35U Vitesse runs, respectively) both with and without negative backgate biases. Two significant observations can be made. First, the Gen. 2 OPFET responsivity is nearly two orders of magnitude lower than the Gen. 3 OPFET responsivity. This is a large run to run variation. Gen. 4 and Gen. 5 OPFET responsivities were similar to the Gen. 3 responsivity and two order of magnitude variations are not typical. Second, this large responsivity difference is correlated with a similar difference in backgate effect sensitivity. The Gen. 2 chip has both low optical responsivity and low backgate effect sensitivity. The Gen. 3 chip, however, has high optical responsivity and a high backgate effect sensitivity. This correlation is expected because both mechanisms rely on the \(p^-\) ion-implanted layer. Figure 3.16 in Subsection 3.2.1 shows a decrease in low optical power responsivity of OPFETs after epitaxial growth. This is equivalent to a decreased backgate effect sensitivity at or below threshold and agrees with the post-growth DFET measurements presented in Figure 5.4. A.C. Grot has suggested that these shifts may be due to an increased concentration of deep level donor states [70]. These deep levels would reduce the backgate \(p^-\) concentration and would explain why the OPFET optical responsivity returns to pre-growth values at high optical intensities (i.e. the empty deep donor states get filled by excited photocarriers). This hypothesis can be tested, by determining the dopant energy, by measuring the OPFET responsivity spectrum [147].

There are at least three methods to reduce the effect of backgating on E-o-E based OEIC devices and circuits. The first method is to include \(p\)-type ohmic contacts in the Vitesse, or another commercial MESFET, process. \(p\)-type ohmic contacts would allow the backgate potential to be fixed at a given bias, nominally \(V_S\). This is similar to CMOS circuits which include \(p\)- and \(n\)-well taps roughly every \(20 \mu\text{m}\) to reduce backgating effects as well as to prevent latch-up. While this is the most obvious solution, it is also the longest term solution because it involves adding process steps
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Figure 5.7: Resistor connected DFET drain-source current ($V_{DS} = 1.0$ V) vs. backgate voltage. The backgate voltage was applied through a standard S/D ion-implanted ohmic metal contact (control pad) and a AuGe/Ni/Au n-type ohmic contact (Gold pad) in a S/D ion-implanted DGW. The GaAs substrate around the gold pad was etched to different depths [70].

to a production line. P-type ohmic contacts have been fabricated at Vitesse [31], for use in high-voltage circuits [75], though there are no known plans to include these steps in the standard process flow.

A second method to reduce the backgating effect is to isolate the p− layer by etching an annular ring around the device or circuit. A trench that extends through the p− layer should effectively isolate the device backgate from the rest of the backgate plane. A.C. Grot tested this method on a Gen. 3 chip. A AuGe/Ni/Au n-type ohmic contact was evaporated in the large S/D n+ ion-implanted DGW region and served as the backgate test contact. A S/D implant with a standard ohmic metal contact served as the backgate control contact. The effect of negative applied biases on each of these contacts, and therefore on the backgate potential, was monitored by measuring the drain-source current through a resistor connected DFET. Figure 5.7 shows the resistor connected DFET drain-source current ($V_{DS} = 1.0$ V) vs. backgate voltage. The backgate voltage was applied through a standard S/D ion-implanted
ohmic metal contact (control pad) and a AuGe/Ni/Au n-type ohmic contact (Gold pad) in a S/D ion-implanted DGW. The control pad and gold pad curves are identical. The GaAs substrate around the gold pad was etched to different depths with H$_3$PO$_4$:H$_2$O$_2$:H$_2$O (1:1:5). Figure 5.7 shows that a $\sim 1$ $\mu$m (between 0.7 $\mu$m and 1.4 $\mu$m) deep trench around the gold pad successfully reduces the influence of gold pad biases on the DFET drain-source current (i.e. backgating effect). This experiment also confirms that the p$^-$ layer depth is roughly 1 $\mu$m. A backgate isolation trench etch could be included in the E-o-E process flow by designing DGW annular rings around devices or circuits. After growth the single crystal material in these rings could be exposed to all wet and dry etches in the standard E-o-E device flow (e.g. polycrystalline material etch, $\sim 4$ $\mu$m, and mesa etch, $\sim 1$ $\mu$m). If the total etch depth is not sufficient to etch $\sim 1$ $\mu$m into the substrate, addition photoresist patterning and etching steps can be added. Annular rings can be thin ($\sim 5$ $\mu$m) and close to the device or circuit to be protected, thereby increasing the area per circuit by a nominal amount. Interconnect metallization across the trench can be achieved by designing interlevel dielectric bridges across the trench (e.g. a bridge across a moat). This bridge can contain metal 1 - metal 3 within the structure and metal 5 can be patterned on top of the bridge. The ultimate reduction in circuit density and design flexibility, introduced by backgate trenches, remains to be experimentally determined. MIT-OEIC-4 also includes several test structures to explore these ideas [126].

The third, and final, backgate effect reduction method is to isolate the p$^-$ layer beneath a device or circuit with annular depletion rings instead of etches. A S/D ion-implanted ring with standard ohmic metal contacts can be designed around devices or circuits. A positive voltage applied to the ring should depleted the p$^-$ layer beneath the ring and thereby isolate backgate on the interior of the ring from backgate surrounding the ring. Figure 5.8 shows a 40 $\mu$m $\times$ 1 $\mu$m (with 10 $\mu$m (source/drain)-to-gate spacings) OPFET drain-source current ($V_{DS} = 1.0$ V) vs. backgate voltage for various guard ring positive biases. The OPFET optical input power was 10 nW
5.2. BACKGATING EFFECT

Figure 5.8: 40 $\mu$m $\times$ 1 $\mu$m (with 10 $\mu$m (source/drain)-to-gate spacings) OPFET drain-source current ($V_{DS} = 1.0$ V) vs. backgate voltage for various guard ring positive biases. The OPFET optical input power was 10 nW and the backgate voltage was applied through a S/D ohmic metal backgate tap outside the guard ring [70].

and the backgate voltage was applied through a S/D ohmic metal backgate tap outside the guard ring. The OPFET responsivity is lower with a 0.0 V biased guard ring than without a guard ring. A guard ring bias of 3.0 V significantly reduces the backgating effect. Figure 5.8 also shows that the OPFET responsivity, and presumably E/D MESFET drain-source currents, is higher at 0.0 V backgate voltage for positive biased guard rings than without a guard ring. This increase ($\sim$30% at 3.0 V) is possibly due to an increased backgate potential which reduces the channel depletion width thereby increasing the drain-source current. Guard rings can be included in the standard E-o-E process flow by designing S/D annular rings with ohmic metal contacts around devices and circuits. Several rings can be connected and routed to a single bond pad where an external bias can be applied (e.g. 3.0 V). This additional bias rail is similar to CMOS well tap rails, though CMOS does not require three different bias rails. MIT-OEIC-3 and MIT-OEIC-4 include several guard ring test structures to further quantify this backgate effect reduction method.
5.3 Bond Pad Protection

Optoelectronic circuit packaging typically requires the chip die to be mounted in a DIP or PGA, with conductive epoxy, and thin bond wires to be connected from the package pin pads to the chip bond pads. Rugged, low resistance bonds between the bond wires and the chip bond pads relies on the bond pads being pliable. Gold ball bonds and aluminum wedge bonds are common and use both use heat and ultrasonic vibrations to adhere the bond wire tip to the chip bond pad, typically aluminum. If the growth temperature is too high (discussed below), the Vitesse HGaAs3 bond pads become hard and cracked and bonding is not possible. Two solutions have been successfully demonstrated and further improvements should be possible.

Bond pad degradation is primarily due to the W-Al reaction previously discussed in Subsection 3.1.1. This conclusion was reached by attempting to bond two MIT-OEIC-1 chips. Chip A was thermally cycled in a furnace for five hours at 530°C. Chip B was coated with \( \sim 2000 \text{ Å} \) of SiO\(_2\) and thermal cycled like chip A, after which the SiO\(_2\) was removed with BOE. Au-ball bonds and Al-wedge bonds did not adhere to either chip A or B. Chip B was a control to verify that the Al chip pads were not oxidizing. An MIT-OEIC-3 chip (S001) was MBE thermal cycled at 470°C for five hours and could be readily bonded. Figure 3.1 in Subsection 3.1.1 indicates that the WN\(_x\) plated Al interconnect line transition from low resistance (no W-Al reaction) to high resistance (W-Al reaction) is centered at \( \sim 500°C \) for five hour thermal cycles. Chips A, B and S001 agree with this prediction and verify that temperature alone is responsible for bond pad degradation.

Two methods to increase the bond pad temperature limit were investigated with MIT-OEIC-3 chips. The first method was to have Vitesse increase the nitrogen concentration in the WN\(_x\) barrier layer beneath metal 4. As shown in Subsection 3.1.1, by raising the nitrogen concentration from 10%-20% to \( \sim 30\%\) the transition temperature, from low resistance (no W-Al reaction) to high resistance (W-Al reaction), can be shifted from \( \sim 500°C \) to higher than \( \sim 550°C \). The MIT-OEIC-3 lot was split
<table>
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<th>530°C</th>
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<tr>
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<td>MIT-OEIC-1 chip with IPSELs</td>
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Table 5.1: Bonding test summary listing MIT-OEIC-3 chip number, description of the cycle and chip conditions, and the percentage of successful Au-ball bonds to Al pads. Standard (S) and increased nitrogen concentration (N) WNx barrier (beneath metal 4) process chips, an additional protective 3700 Å low-stress SiOₓNᵧ layer [52] and Cr(245 Å)/Au(2400 Å) layers were included in this test. Growths/thermal cycles of 5-hour duration were conducted at temperatures of 470°C, 490°C, 530°C and 550°C.
Figure 5.9: 400× optical photograph of an S001 bond pad after a five-hour, 470°C thermal cycle.

to produce a standard lot (S) and an increased nitrogen concentration in the WN$_x$ barrier layer beneath metal 4 (N). The second method was to evaporate Cr/Au on the bond pads after the thermal cycle [63]. The Cr/Au should make good electrical contact while providing a soft surface for bonding.

Table 5.1 summarizes the preliminary bond pad tests. The table lists the MIT-OEIC-3 chip number, a description of the cycle and chip conditions, and the percentage of successful Au-ball bonds to Al pads. Standard (S) and increased nitrogen concentration (N) WN$_x$ barrier (beneath metal 4) process chips, an additional protective 3700 Å low-stress SiO$_x$N$_y$ layer [52] deposited before growth and removed after growth with BOE, and Cr(245 Å)/Au(2400 Å) layers were included in this test. Growth/thermal cycles of 5-hour duration were conducted at temperatures of 470°C, 490°C, 530°C and 550°C.

S001, N007 and N008 chip bond pads could all (100%) be bonded. Figures 5.9 and 5.10 are 400× optical photographs of a S001 and N007 bond pads after a five-hour, 470°C thermal cycle and growth, respectively. Both pads show circular features not
Figure 5.10: 400× optical photograph of an N007 bond pad after a five-hour, 470°C growth cycle.

Figure 5.11: 200× optical photograph of N007 RTD-based SRAM circuit bond pads after a five-hour, 470°C growth cycle. Au-ball bonds appear on the six bond pads.
present previous to thermal cycle or growth. The N007 chip shows additional circular features which could be residual polycrystalline material not removed by the poly-strip etch. Both pads are easily marked with probe tips and appear to be in excellent condition. Figure 5.11 is a 200× optical photograph of N007 RTD-based SRAM circuit bond pads after a five-hour, 470°C growth cycle. Au-ball bonds appear on the six bond pads. An MBE growth on an S series chip should be conducted. N008 had a SiO$_x$N$_y$ layer deposited before growth to serve as a control for an Al-GaAs interaction, which could be present on the N007 chip. Unfortunately, a brown reside, possibly Al-N [52], appeared on the N008 bond pads after the SiO$_x$N$_y$ layer was removed with BOE. The residue did not prevent bonding.

N006 and N009 chip bond pads could be bonded with a success rate of 100% and ~20%, respectively. The N006 result indicates that N series bond pads can survive beyond 530°C, which was previously shown to cause complete bonding failure for MIT-OEIC-1 chips (i.e. S series). Figure 5.12 shows a 400× optical photograph of N006 bond pad after a five-hour, 470°C thermal cycle. The bond pad appears
5.3. **BOND PAD PROTECTION**

to have either reacted or lost Al (pits) and the dielectric stack is cracked (typically observed for temperatures beyond 530°). A Au ball bond appears on the lower-right pad. The pad morphology should improve at lower temperatures. The N006 chip also suggests that a brief period at 550°C, to thermally desorb the native oxide, followed by a growth at 470°C should be possible with N series chips. N009 had a brownish residue, identical to that on N008, which presumably reduced the bonding success rate.

The final MIT-OEIC-3 chip tested was N002. RTDs were grown on this chip after spending seven minutes at 610° to simulate an aggressive native oxide desorption period. No pads could be bonded after this growth (polycrystalline material was stripped). By evaporating Cr/Au on the pads, however, ~75% of the pads could be bonded. While ~75% is not an acceptable rate, this result does indicate that Cr/Au can adhere to the bond pads, when the Au ball can not, and provides a supple surface for the Au ball. The bonding success rate is expected to be higher for chips that have the native oxide thermally desorbed at 580°C for five minutes (e.g. lower temperatures). The total contact resistance with the Cr/Au layer has not been measured. For reference, an MIT-OEIC-1 chip (##44 and S series like) with fully processed integrated IPSELS is listed to indicate that it could not be bonded.

Bonding does not appear to be a problem for growth temperatures of 470°C or below. Hydrogen plasma native oxide removal and either low-temperature (In,Al,Ga)As or (In,Ga)AsP growths are required to keep within the 470° temperature limit. Brief periods (e.g. minutes) at 550°C to thermally desorb the native oxide also appears to be possible with N series chips. The future of N series chips is uncertain. Vitesse has found that the resistance of the ~30% WN_x layers is roughly two orders of magnitude higher than the 10%-20% WN_x resistance [31]. This prevents increased nitrogen concentration WN_x barrier from being used lower in the dielectric stack (e.g. between metal 1 and ohmic metal) because dimensions are typically smaller and the absolute resistance increase is more significant. Alternate barrier materials are being
investigated for increased thermal stability properties [31].

5.4 Multi-Project Chip (OPTOCHIP)

As the E-o-E based OEIC technology has developed, numerous optical systems groups have inquired about accessing this technology. In response to this interest, a multi-project (multi-user) E-o-E based OEIC chip termed OPTOCHIP has been proposed, funded and scheduled. Fonstad's group at MIT, which is the NCIPT E-o-E OEIC project coordination center [125], will serve as the OBP “drop in” cell design and project coordination center for OPTOCHIP. Additional project infrastructure will be provided by the ARPA/NSF Consortium for Optical and Optoelectronic technologies for Computing (CO-OP). The OPTOCHIP offering is viewed as the first step in the establishment of a formal mechanism by which users can have regular access to the E-o-E technology and through which E-o-E researchers and developers can interact with the user community.

Figure 5.13 is a schematic illustration of the OPTOCHIP layout. Each user group will receive one 2.5 mm × 2.5 mm sub-chip (eight total, 1-4 and 6-9) for OEIC design. OBP “drop in” cell designs (see Subsection 4.8.1) will be provided to the user groups by MIT. The nine sub-chips will be arrayed at MIT. Process control monitor OEICs (5), a 1 mm × 1 mm DGW (a) for in-situ RHEED growth monitoring, a photoresist edge buildup cuff (b), and saw lanes (c) will also be added at MIT. OPTOCHIP will be fabricated at MOSIS/Vitesse, LEDs will be epitaxially grown at MIT and the LEDs will be E-o-E processed at MIT/MTL. The sub-chips will be distributed to user groups following dicing.

User group OEICs will include VLSI GaAs E/D MESFET circuits, standard process OPFETs, standard process MSMs and E-o-E integrated LEDs. OBP “drop in” cells are currently being designed and tested (see Sections 4.7 and 4.8). OPTOCHIP user design workshops (via the network) are scheduled for summer 1995,
MOSIS/Vitesse fabrication is scheduled for fall 1995 and E-o-E LED integration is scheduled for winter 1996.

Figure 5.13: Schematic illustration of the OPTOCHIP layout. Each user group will receive one 2.5 mm × 2.5 mm sub-chip (eight total, 1-4 and 6-9) for OEIC design. OBP "drop in" cell designs will be provided to the user groups by MIT. The nine sub-chips will be arrayed at MIT. Process control monitor OEICs (5), a RHEED DGW (a), a photoresist edge buildup cuff (b), and saw lanes (c) will also be added at MIT. OPTOCHIP will be fabricated at MOSIS/Vitesse, LEDs will be epitaxially grown at MIT and the LEDs will be E-o-E processed at MIT/MTL. The sub-chips will be distributed to user groups following dicing.
Appendix A

LED Fabrication Flow

This appendix contains a detailed description of the LED fabrication flow for both E-o-E integrated LEDs and LEDs on bulk epitaxy (skip first nine steps).
MIT OEIC Chip #: _____

Electrical characterization: _____

1. Dielectric stack

- Silicon Nitride (10000A)
- Silicon Dioxide (8000A)
- SOG (4000A)
- Silicon Dioxide (4500A)
- Silicon Dioxide (4300A)
- SOG (2000A)
- Silicon Dioxide (4500A)
- Silicon Dioxide (4600A)
- Silicon Nitride (350A)
- n+ S/D implant

4.225 um total

Epi-window clean:

RIE (10m, 45 sccm CF4, 10 sccm O2, 50mT, 200W): _____

BOE (5m, ultrasonic): _____

Electrical characterization: _____

2. Vitesse epi-window RIE

RIE

100 um
3. MBE growth

- p⁺ GaAs cap (1000Å)
- p Al(0.3)Ga(0.7)As (7000Å)
- p⁺ GaAs (6000Å)
- n Al(0.3)Ga(0.7)As (3000Å)
- n⁺ GaAs buffer (25000Å)
- n⁺ GaAs/AlGaAs S.L.

MBE growth:

- Degrease (TCA, Acetone, methanol, DIH2O):
- Mount (Indium):
- Growth #:
- Dismount (Indium):
- Backside indium removal (black wax, 1:1 HCl:DIH20, 90C):
- Degrease (TCA, Acetone, methanol, DIH2O):

4. Planarize with PR

- Planarize with PR:
- Spin (S1400-31, 40s, 4 Krpm):
- Hotplate (70s, 100C):
Planarization Lithography:

Expose on Karl-Suss 1:1 (Planarization mask, ~70s):

Develop (S319, 20s):

Polycrystalline etch (5:1:1 DIH20:H2O2:H3PO4, ~2m):
PR strip:
Acetone:
Propanol:
Plasma ash (5m, He(3%)O2, 1T, 50W):

OR

Acetone:
Methanol:
DIH2O:
Plasma ash (5m, O2, .1T, 100W):

Electrical characterization:
Mesa lithography:

Spin (AZ 5214E, 30s, 5 Krpm):

Hotplate (90s, 115C):

Expose on Karl-Suss 1:1 (IBAE1 mask, 10s):

Develop (AZ327, ~2m 15s):
Mesa etch (IBAE):
Etch 1.70 um:

OR

Mesa etch (wet chemical):
Etch 1.70 um (1:1:6
H3PO4:H2O2:Acetic acid
at ~ 1.5 um/m):

PR strip:
Acetone:
Propanol:
Plasma ash (5m, He(3%)O2,
1T, 50W):

OR

Acetone:
Methanol:
DIH20:
Plasma ash (5m, O2, .1T, 100W):
13. Dielectric deposition

Dielectric deposition (PECVD):

PECVD SiO2 (1000A):

OR

Dielectric deposition (sputter):

Sputter SiO2 (1000A):

14. Pad dielectric lithography

Pad dielectric lithography:

Spin (AZ 5214E, 30s, 5 Krpm):

Hotplate (90s, 115C):

Expose on Karl-Suss 1:1
(Pad-strip mask, 10s):

Develop (AZ327, ~2m 15s):
Pad dielectric etch:

BOE etch (1000Å, ~1m):

---

PR strip:

Acetone: 

Propanol: 

Plasma ash (5m, He(3%)O₂, 1T, 50W):

---

OR

Acetone: 

Methanol: 

DIH₂O: 

Plasma ash (5m, O₂, 1T, 100W): ---
Via cut lithography:
Spin (AZ 5214E, 30s, 5 Krpm):
Hotplate (90s, 115C):
Expose on Karl-Suss 1:1
(Via cut mask, 10s):
Develop (AZ327, ~2m 15s):

Via etch:
BOE etch (1000A, ~1m):
19. PR strip

PR strip:
Acetone:
Propanol:
Plasma ash (5m, He(3%)O2, 1T, 50W):

OR

Acetone:
Methanol:
DIH2O:
Plasma ash (5m, O2, .1T, 100W):

P-metal lithography:
Spin (HMDS, 40s, 5.5 Krpm):
Spin (S1400-27, 40s, 5.5 Krpm):
Oven bake (30m, 90C):
Chlorobenzene soak (90s):
Oven bake (5m, 90C):
Expose on Karl-Suss 1:1 (P-metal mask, 5s):
Develop (MF319, ~70s):

20. P-metal lithography
21. Au/Zn metallization

Au/Zn metallization:
- Plasma ash (45s, O2, .1T, 100W):
- BOE dlp (3s):
- DIH2O:
- Evaporate (12Khz, ~2500A):

22. P-metal liftoff

P-metal liftoff:
- Ultrasonic acetone (~20m):
- Methanol:
- DIH2O:

Au/Zn anneal:
- RTA (15s, 420C):

Optoelectronic characterization:
Appendix B

IPSEL Fabrication Flow

This appendix contains a detailed description of the IPSEL fabrication flow for both E-o-E integrated IPSEls and IPSEls on bulk epitaxy (skip first nine steps).
MIT OEIC Chip #:

Electrical characterization:

4.225 um total

Silicon Nitride (10000A)
Silicon Dioxide (8000A)
SOG (4000A)
Silicon Dioxide (4500A)
Silicon Dioxide (4300A)
SOG (2000A)
Silicon Dioxide (4500A)
Silicon Dioxide (4600A)
Silicon Nitride (350A)
n+ S/D implant

1. Dielectric stack

Epl-window clean:
RIE (10m, 45 sccm CF4, 10 sccm O2, 50mT, 200W):
BOE (5m, ultrasonic):

Electrical characterization:

2. Vitesse epl-window RIE
3. MBE growth

Photo Resist

4. Planarize with PR

MBE growth:

Degrease (TCA, Acetone, methanol, DIH2O):

Mount (Indium):

Growth #:

Dismount (Indium):

Back-side Indium removal (black wax, 1:1 HCl:DIH20, 90C):

Degrease (TCA, Acetone, methanol, DIH2O):

Planarize with PR:

Few drops Microposit primer:

Spin (30s, 30s, 4Krpm):

Spin (AZ 4620, 30s, 30s, 4Krpm):

Hotplate (15m, 95C):
Planarization Lithography:

Expose on Karl-Suss 1:1 (Planarization mask, 5m):

Develop (9:1 DIH2O:AZ303):

5. Planarization PR

Polycrystalline etch (5:1:1 DIH2O:H2O2:H3PO4, ~2m):

6. Polycrystalline etch
PR strip:

Acetone:

Propanol:

Plasma ash (5m, He(3%)O2,
1T, 50W):

7. PR strip

Electrical characterization:

8. Longitudinal view
9. Lateral view

10. Vertical mirror PR

Vertical mirror lithography:

Spin (AZ 5214E, 30s, 5 Krpm):

Hotplate (90s, 90C):

Expose on Canon 4:1 (flood, setting 1.0):

Hotplate (90s, 115C):

Expose on Canon 4:1 (IBAE1 mask, setting 8.11):

Develop (AZ327):
Vertical mirror etch:

Preclean (Ar beam, 2m):

IBAE etch (3 um):

PR strip:

Acetone:

Propanol:

Plasma ash (5m, He(3%)O2, 1T, 50W):

Parabolic mirror lithography:

Spin (AZ 1375, 30s, 5 Krpm):

Hotplate (10m, 90C):

Expose on Karl-Suss 1:1 (IBAE2 mask, 2m):

Develop (9:1 DIH2O:AZ303A):

Oven (20m, 120C):
Parabolic mirror etch:

Preclean (Ar beam, 2m):

IBAE etch (prog. coscut):

PR strip:

Acetone:

Propanol:

Plasma ash (5m, He(3%)O2, 1T, 50W):

13. Parabolic mirror etch

14. Lateral view
15. Longitudinal view

Ridge waveguide lithography:
Spin (AZ 1375, 30s, 5 Krpm):
Hotplate (10m, 90C):
Expose on Karl-Suss 1:1 (IBAE3 mask, 1m):
Develop (9:1 DIH2O:AZ 303A):
Oven (20m, 120C):

16. Ridge waveguide PR
17. Ridge waveguide etch

18. Longitudinal view

Ridge waveguide etch:

Preclean (Ar beam, 2m):

IBAE etch (2.1 um):

PR strip:

Acetone:

Propanol:

Plasma ash (5m, He(3%)O2, 1T, 50W):
19. SiO2 PECVD & pattern

20. P-contact SiO2 RIE PR

SiO2 PECVD:
0.507 um (SiO2, 275C):

SiO2 pattern lithography:
Spin (AZ 1375, 30s, 5 Krpm):
Hotplate (10m, 90C):
Expose on Karl-Suss 1:1 (PECVD mask, 1m):
Develop (9:1 DIH2O:AZ 303A):
Oven (20m, 120C):
SiO2 etch (B-HF, ~30s):
PR strip:
Acetone:
Propanol:
Plasma ash (5m, He(3%)O2, 1T, 50W):

P-contact SiO2 RIE lithography:
Spin (AZ 1375, 30s, 5 Krpm):
Hotplate (10m, 95C):
Expose on Karl-Suss 1:1 (RIE mask, 2m):
Develop (9:1 DIH2O:AZ 303A):
Oven (20m, 120C):
P-contact SiO2 RIE:
RIE (CF4, 250V, ~28W, 52m):

PR strip:
Acetone:
Propanol:
Plasma ash (5m, He(3%)O2, 1T, 50W):

P-metal lithography:
Few drops of Microposit primer:
Spin (30s, 30s, 4Krpm):
Spin (AZ 4620, 30s, 30s, 4Krpm):
Hotplate (15m, 95C):
Exposure on Karl-Suss 1:1
(p-metal mask 1, 2.2m):

P-metal angle evaporation:
Mount (15/° degree angles):
Au/Zn (°):
P-metal liftoff:
Acetone (soak):
Propannl:
Plasma ash (5m, He(3%)O2, 1T, 50W):

23. Final longitudinal view

Optoelectron\textsuperscript{r} characterisation:

24. Final lateral view
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