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Introduction to semiconductor processing: Fabrication and characterization of *p-n* junction silicon solar cells

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We describe an upper-division undergraduate physics laboratory experiment that integrates the fabrication and characterization of a *p-n* junction in silicon. Under standard illumination, this *p-n* junction exhibits the photovoltaic effect as well as the typical diode rectification behavior when measured in the dark. This experiment introduces students to the physics of solar photovoltaics from the perspective of participating in the fabrication process. Procedures, experimental strategies, and typical student measurement results are presented. This low-cost, engaging, and effective lab can be adapted to undergraduate physics courses at various institutes.
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I. INTRODUCTION

Given the present-day challenges of climate change and depleting reserves of fossil fuels, there is international focus on the development of efficient, clean sources of renewable energy. For the previous two decades, the photovoltaics sector has been the fastest growing industry of its size at an annual rate of ∼40%.[1] Moreover, the techniques for fabricating silicon solar cells are connected with those for fabricating electronic devices that are ubiquitous in our modern age.

College students are often familiar with renewable energy in the context of climate change and energy security; however, physics education at the university level does not always connect the practical idea of using the physical properties of semiconductors to harness energy from the Sun. Furthermore, this experiment draws on the interdisciplinary nature of science technology, engineering and mathematics (STEM) fields such as materials science where a thorough understanding of multiple concepts is needed. This laboratory provides opportunities for students to understand semiconductor fabrication and characterization, a general process which is the subject of much research and development in a wide range of technologies for computation, communications, sensing, etc. The techniques explored here provide students with an important educational experience regarding the process by which electronic devices are manufactured as well as critical-skill development for future careers in STEM fields.

Several excellent educational articles on solar cells have been published in the past 40 years, including understanding the solar cell from an equivalent circuit model[2–5] and fabricating dye-sensitized solar cells in the lab.[6] We build on these techniques by presenting a modernized experimental approach that integrates the experience of semiconductor fabrication and measurement to improve student understanding of what goes into creating a solar cell and how it functions and performs. By combining these topics, we hope to educate students in modern topics that bridge physics with societal and economic issues.

The complete experiment of solar cell fabrication and characterization can be comfortably carried out in 4 experimental sessions over a period of 2 weeks. The cost of materials for a lab of up to 30 students is less than $300, assuming that access to an annealing furnace and a facility for performing the hydrofluoric acid (HF) etch are available. In our first session, we spin-coated and annealed the silicon wafers. The second session involved etching the wafer in HF acid, which presented an opportunity for a site visit to the Stanford Nanofabrication Facility (SNF) to perform this step. While a visit to such a facility is not necessary for performing the etching step, university safety regulations prevent us from using HF acid on campus. SNF is one of nearly twenty National Science Foundation-funded National Nanotechnology Coordinated Infrastructure (NNCI) sites located throughout the United States whose mission includes outreach opportunities such as our class visit. This visit engaged our students in an experience of entering a cleanroom nanofabrication facility as well as learning about modern nanofabrication techniques. Our third session involved attaching electrical contacts to finalize our solar cell devices. Finally, we measured the current vs. voltage (IV) characteristics of our *p-n* junctions, ultimately extracting important materials parameters such as the solar cell's open-circuit voltage (V_{OC}), the short-circuit current (I_{SC}), and a full IV curve under both light and dark conditions, the latter displaying the typical diode rectification curve. Several supplementary exercises are suggested in this paper, engaging students in understanding common procedures used in the semiconductor industry and interpreting results for their own fabricated solar cells.

II. THEORETICAL BACKGROUND

A. The solar cell as a *p-n* junction

The diode (including the light-emitting diode) and the solar cell are silicon-based devices with similar fabrication processes and structure. Intentionally adding impurity "dopant" atoms to silicon in small concentrations can modify the electrical properties of the crystal, allowing the formation of a *p-n* junction. Dopants with more valence electrons than the four that silicon has (e.g., phosphorous with five valence electrons) are *n*-type dopants, the *n* referring to the extra

"negative" electron contributed. Dopants with fewer valence electrons than silicon (e.g., boron with three valence electrons) are *p*-type dopants, the *p* referring to the absence of the electron—i.e., a "positive hole" that this type of impurity contributes to the material. Joining *n*-type doped silicon and *p*-type doped silicon form a *p*-*n* junction, the basic structure of both the diode and the solar cell.

Since many articles and books are written on the physics of the *p*-*n* junction,[7–9] we will present only the most basic model used to describe the current and voltage response of a solar cell. The physics of the *p*-*n* junction is also important to understanding transistors, the fundamental building blocks of modern computers. By independently fabricating and characterizing *p*-*n* junctions, students build a solid foundation to better understand other semiconductor devices.

When illuminated with light, the *p*-*n* junction can drive a current, operating as a solar cell. There are two fundamental currents generated at the *p*-*n* junction: the drift current and the diffusion current, which flow in opposite directions. Under "dark" conditions (i.e., when the solar cell is not in sunlight), these currents balance each other and no net current flows. At the microscopic level, the drift current originates from the internal electric field created at the interface of the *p*-type and *n*-type silicon. The diffusion current originates from the disparate carrier concentrations in the *n*-type and *p*-type regions, with electrons tending to diffuse from the higher electron concentration region found in the *n*-type silicon towards the lower electron concentration region found in the *p*-type silicon. Similar action, though in the opposite directions, occurs for the holes.

Under illumination, the drift current becomes greater than the diffusion current, so that when a load is attached to the solar cell, a current is produced in the opposite direction to the conventional flow of current in a standard diode. In a band theory model, absorbed photons excite more carriers into the conduction band where they are then free to enter the region of electric field and pick up a drift velocity.

A solar cell can be compared with a battery, with its similar functionality and the ability to connect both solar cells and batteries in parallel or series. However, batteries are effectively a source of constant voltage with the current varying with respect to its load, whereas a commercial solar cell behaves as a constant current source for low-resistance loads. The fundamental response of a solar cell can be modeled by the circuit shown in Fig. 1(a), including a constant light-generated current source, I_L, series resistance, R_S, shunt resistance, R_{sh}, and a diode, yielding a transcendental equation in I, as worked out in Ref. 10

$$I = I_L - I_0\left[\exp\left(\frac{qV + IR_S}{Ak_BT}\right) - 1\right] - \frac{V + IR_S}{R_{sh}}, \tag{1}$$

where I_0 is the dark saturation current (which for good panels is typically quite low, $\sim 10^{-8}$ A), q is the electronic charge in Coulombs, k_B is the Boltzmann constant, T is the temperature in Kelvin, and A is an "ideality" factor (typically ~ 1).[2,11] The short-circuit current, I_{SC}, measured with zero-resistance load ($V \to 0$), is approximately I_L for low enough R_S and large R_{sh}. In fact, for a high-efficiency solar cell with $R_S \to 0$ and $R_{sh} \to \infty$, this equation reduces to the analytic expression

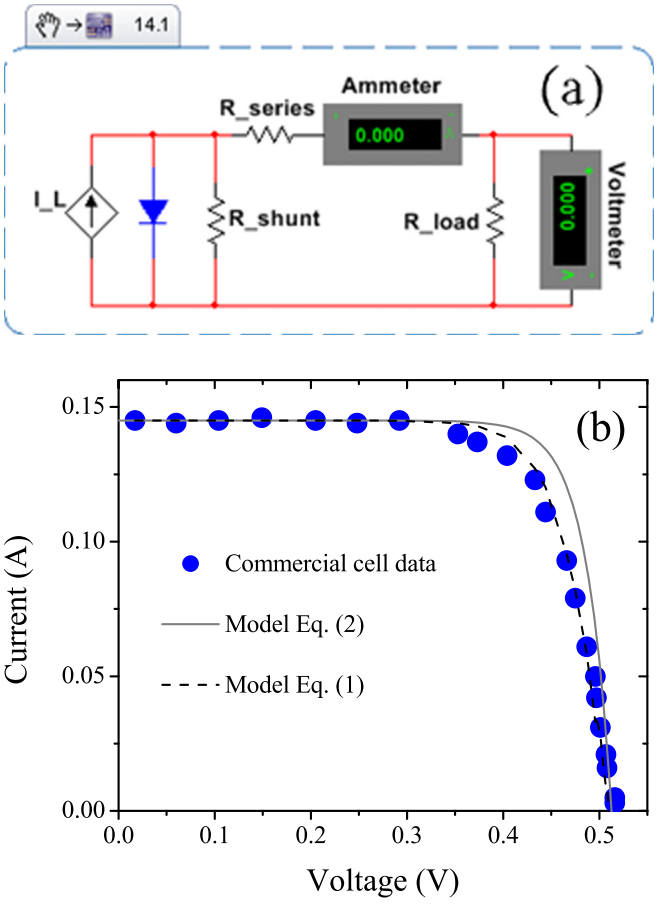

Fig. 1. (a) The equivalent circuit ("snippet" from National Instruments Multisim) used to model and measure solar cell characteristics, where R_series (R_S), R_shunt (R_{sh}), and R_load (R_L) are as in Eq. (1). (b) Student-measured IV curve data for a commercial mini solar panel with fits using the circuit models discussed in the text. Dashed line fit is Eq. (1) using $R_S = 0.2\ \Omega$ and $1/R_{sh} = 0$.

$$I = I_{SC} - I_0\left[\exp\left(\frac{qV}{Ak_BT}\right) - 1\right], \tag{2}$$

allowing the current and voltage relation to be plotted directly as in Fig. 1(b). We may also discover the open circuit voltage, V_{OC}, measured with a large load resistance, by setting $I \to 0$, yielding typically 0.5–0.6 V.

Using a variable irradiance method,[2] students determined R_S for the commercial mini panel to be approximately 0.2 Ω. Using this value for R_S, the Eq. (1) model curve in Fig. 1(b) indicates that even the addition of this small parasitic series resistance in the analysis improves the fit for a commercial solar cell data.

B. Physics of diffusion doping

We now discuss the novel aspect presented in this experimental lab, which is a fundamental process used in the semiconductor industry—making the *p*-*n* junction—by a process known as diffusion doping, driving impurity atoms into the Si wafer through annealing at high temperatures. The physics of the diffusion process for impurity atoms is analogous to that of diffusion of charge carriers, where here it is dopant *atoms* that diffuse permanently into the silicon wafer. For our experimental procedure, we provide students with a boron-doped wafer. They then use a spin-on dopant (SOD),

which is an oxide that contains (n-type) phosphorous in a solvent solution that is spun-cast onto the p-type wafer then left to dry.[8] Placing the coated wafer into an annealing furnace drives the phosphorous atoms via diffusion into the p-type wafer.[12] The flux, F, of dopant atoms passing through a unit area per unit time is $F = -D\frac{\partial n}{\partial x}$, where D is the diffusivity and n is the dopant concentration per unit volume. For low concentrations of doping atoms, D is independent of n and the one-dimensional continuity equation leads to Fick's Diffusion Equation.[7] Using the boundary condition of a constant surface dopant concentration—i.e., the solid solubility limit of phosphorous, which is exceeded in the SOD—and using the diffusivity of phosphorus in silicon for our anneal temperature (at 925 °C, $D \cong 1 \times 10^{-15}\text{cm}^2/\text{s}$),[7] one can model the doping depth profiles for different annealing times as shown in Fig. 2 using the following complementary error function solution:

$$n(x,t) = n_S \,\text{erfc}\left(\frac{x}{2\sqrt{Dt}}\right), \tag{3}$$

which describes the concentration of n-type dopant as a function of depth, x, into the wafer after annealing for a time, t, and $n_S = 3 \times 10^{20}\,\text{cm}^{-3}$ is the dopant concentration in the SOD film and also the solid solubility limit of phosphorous in silicon.

At high temperatures, the phosphorous atoms diffuse into the p-type wafer. After cooling, the wafer's front side has a higher concentration of phosphorous atoms as compared to boron atoms, such that the front side is considered n-type doped. When both an n-type and p-type dopant are present in a region of silicon, the type of dopant with the higher concentration provides the majority of the carriers, determining the designation as n- or p-type. After the diffusion process, we note that the resulting concentration of the phosphorous atoms drops rapidly as a function of depth, as seen in Fig. 2. We mark the depth where the n-type concentration drops below the p-type concentration level of the bulk wafer at 20 min of annealing time, which for this analysis occurs at

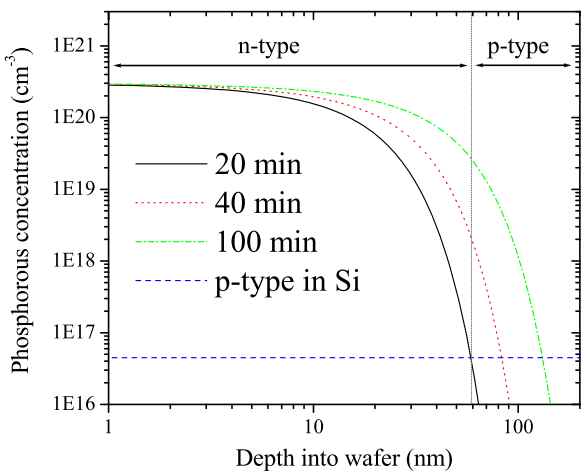

Fig. 2. Increasing the annealing time for the phosphorous-coated Si wafer at 925 °C deepens the n-type region in the wafer. The dashed line represents the threshold level for the p-type dopant, as measured by four-probe on the original boron-doped Silicon wafer. We indicate the n- and p-type regions for a 20 min anneal below the plotted curves. Conventional forward-bias current flow for a diode is in the direction from p- to n-type, whereas for the solar cell under illumination, current flows in the opposite direction.

~60 nm. It is in this crossover region that the depletion layer forms. It is important to note that the crossover between n-type and p-type silicon is quite close to the front surface of the silicon wafer. This closeness is fundamentally necessary as the intensity of the light that enters the silicon decays exponentially with depth according to the skin effect. The depth at which the photons penetrate the material (~100 nm for visible light into Si strongly doped with P atoms) determines the region where electron-hole pairs are created. These electron-hole pairs naturally diffuse until recombination occurs, and only if they enter the depletion region prior to recombining do they then contribute to the drift current.[7,13] Thus, having the junction depth close to the front surface is required for efficient solar cell architectures.

III. METHODS OF SOLAR CELL FABRICATION

The experimental lab described here is an exercise in making a p-n junction starting with a commercial silicon wafer. Simply put, students are handed a bare silicon wafer and create a p-n junction as an end product. By applying metallic contacts and leads, the students are able to then test these functional devices, observing the classic rectification behavior of a diode and the solar cell photovoltaic effect. We describe our procedure below and list equipment used and alternatives in Subsection A1 of the Appendix.

We purchase a p-type silicon wafer, (100) orientation, doped with boron atoms, with a room temperature resistivity in the range of 0.1–1.0 Ω · cm, one-side polished (1SP). A phenomenological correlation between the resistivity and the dopant concentration indicates that the resistivity range corresponds to a boron concentration of $2.8 \times 10^{17} - 1.5 \times 10^{16}\,\text{atoms/cm}^3$, respectively.[14] As an extension project, students experimentally determine the actual room temperature resistivity using a four-probe technique, verifying that it falls in the specified range.[15]

To create the p-n junction, the polished side of a p-type silicon wafer needs to be doped with an n-type dopant, e.g., phosphorous, which was accomplished by the thermally driven diffusion doping process described above. A spin-on film containing a phosphorous-based compound (Filmtronics, Inc. Spin-On Dopant P509) with a phosphorous concentration of 3×10^{20} per cm^3 was used. The viscosity of P509 is quite low, and the material wets readily to silicon surface. Approximately 1 ml of P509 covers a four-inch diameter wafer, yielding an estimated ~1000-nm thick film. A spin speed should be selected which minimizes the lip that builds up at the edge of the wafer. In 10–15 s of spinning, the film will be formed. We found that a sequence of speeds at 30 s each—800, 1500, then 1800 rpm—was appropriate for spreading the liquid uniformly. While we used a Laurell Technologies spin coater, students can build a home-made unit with a standard CPU cooling fan.[16]

For the dopant diffusion step, we used a Lindberg/Blue box furnace (non-vacuum) and annealed the spin-coated wafers at 925 °C for 20 min. The annealing furnaces are used by CSUEB's engineering department for annealing iron rods that are subsequently used for stress testing. This type of annealing furnace is relatively common for colleges and universities that have a materials science or engineering program, making this experimental procedure widely applicable. However, because the annealing furnace is used to anneal iron, residual iron contaminants diffuse into our silicon, forming possible deep-level traps in semiconductor devices that are detrimental to creating high performance

silicon-based devices such as MOSFETs.[17] Thus, though the borrowed annealing furnace was cost effective, the iron contamination contributes to the poor measured performance of our *p-n* junctions by augmenting series resistance, as discussed in our results section.

After the high-temperature diffusion-doping process, the remaining oxide layer must be removed by etching in a diluted HF acid solution, also referred to as a buffered oxide etch (BOE), before electrical contacts can be made across the *p-n* junction. It may be argued that the transparent ~1000-nm thick oxide layer could simply be "scratched" away in the location where we want to apply contacts, thus skipping the etching step. However, this approach is likely to also scratch past the ~60-nm *n*-type layer, making an undesired electrical contact, i.e., a low shunt resistance, with the *p*-type material. If this happens, there will be no voltage difference between the front- and back-contacts, rendering the solar cell unusable. As chemical safety procedures on our campus prevent the use of HF acid, we searched for another option for this step. Since BOE is a standard industry process, coordination of a student visit to either a local university or national facility allows the safe completion of the oxide etch. As mentioned in the Introduction, we coordinated a visit to the Stanford Nanofabrication Facility (SNF) for this purpose.

Measuring the thickness of oxide films using ellipsometry, a common industry tool, can be helpful for monitoring the fabrication process.[18] Prior to our visit to the nanofabrication facility, the students used a spectroscopic ellipsometer to measure the thickness of the oxide layer to better estimate the etch time required for the ~1000-nm thick layer to be completely etched away. After etching, students may also perform a four-point probe measurement to determine the *n*-type layer resistivity and ensure that the oxide layer has been removed. Additionally, this measurement provides an indirect estimate of the *n*-type layer thickness (t), which can be estimated through the relation $\rho = 4.532 \cdot t \cdot (V/I)$, where ρ is the resistivity, and (V/I) is the resistance measured by four-point probe.[19]

With the full-size etched wafer still intact, other side projects designed to teach students standard industry techniques can be included, depending on the availability of equipment. For instance, our students use the spin coating technique to prepare and test an antireflective coating on the solar cells, measuring an increased efficiency by adding the antireflection coating. If a thermal evaporator is available, students can deposit aluminum onto the back side of the wafer to improve electrical contact, also yielding improved efficiency.

At CSUEB, students completed the device fabrication by cleaving the wafer into pieces and applying electrical contacts to each sample. We cleaved the wafers into ~2 cm square samples through a standard scribe-and-cleave technique using a diamond scribe. Cleaving angles tell us about bonding angles in the crystalline structure, e.g., for (100) oriented Si, the angles will be at 90°, and scribing lines perpendicular or parallel to the primary flat or secondary flat will result in a clean cleave.

Making metallic contacts to silicon can be difficult.[20] The simplest approach is an application of silver paint on either side of the sample in a patterned fashion, illustrated in Fig. 3. Thin wires (32-gauge or higher) are then bonded to the wafer by silver paint or "cold-pressing" indium/wire contacts on both sides of the wafer, both producing similar results.

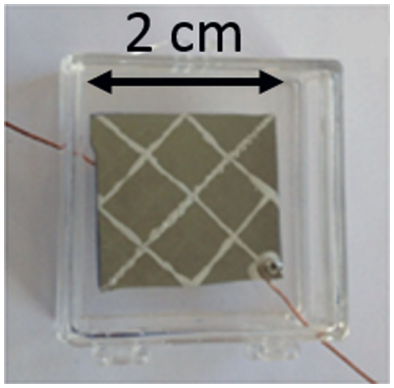

Fig. 3. Photo of a finished silicon solar cell made by a CSUEB student. Solar cell shows the silver paint front contact pattern and is housed in a transparent sample box to provide strain relief for the wires connected to the front (n-type) and back (p-type) surfaces.

IV. MEASUREMENTS OF SOLAR CELL PERFORMANCE

After solar cell devices have been fabricated, we characterized our solar cells alongside commercial miniature solar panels. The comparison with the commercial panels allows calibration of irradiance and deeper insight into the physics of solar cell function. We provide a list of equipment used as well as some optional equipment for extension projects in Subsection A2 of the Appendix.

A. IV curve under illumination

While it can be exciting to measure electricity produced by solar cells outdoors, we found that "bringing the sun inside" using illumination by a lamp can be a good way to carefully characterize the solar cell. To ensure consistent conditions, we used flood lamps with 65 W bulbs at a distance of ~30 cm from the solar cell. The flood lamp provides ~20 mW/cm^2 of irradiance onto the solar cell (a factor of 5 lower than standard AM1.5 peak solar irradiance, 1 kW/m^2 = 100 mW/cm^2).[21] Students used a decade resistor box in parallel with the solar cell as a variable load (ranging from 0.1 Ω up to 200 Ω), while measuring the voltage drop across the cell as well as the series current (connections shown in Fig. 1(a)) to determine current vs. voltage curves and subsequently power vs. voltage curves, as shown in Figs. 4 and 5. Numerous other techniques and further details are described in the literature to measure characteristics of solar cells.[2–4,6,22,23] The range of load resistances required for different size cells will vary, and a potentiometer can be used in lieu of a decade resistance box. Leaving the illumination conditions the same, we repeated the measurement for our fabricated *p-n* junction solar cell samples. For better comparison between different sized solar cells, we plot the current density, $J = I/A$, where A is the surface area of each solar cell. Using the variable irradiance method,[2] we also determined an approximate value for the series resistance, R_S.

B. IV curve under dark conditions

While the previous measurement can be sufficient for a shorter lab activity, further exploration helps students to realize that the "solar cell" is fundamentally a *p-n* junction and allows determination of other factors that affect solar conversion efficiency, e.g., the parasitic resistances.

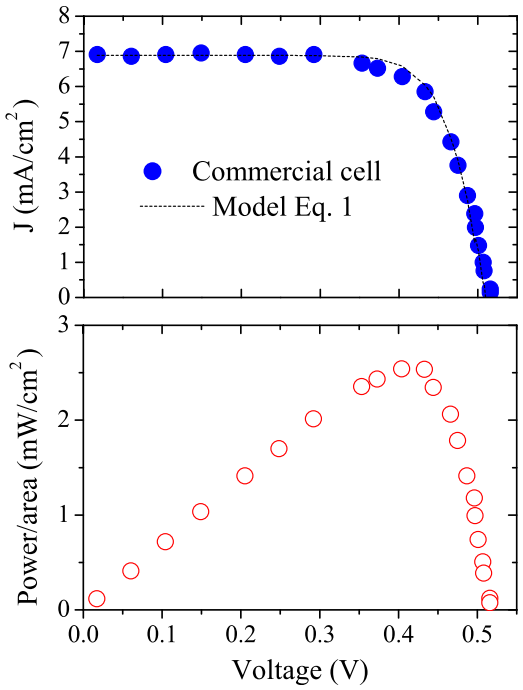

Fig. 4. JV curve for the commercial mini solar panel (area 21 cm^2) along with the associated power curve. Fit is Eq. (1) using $R_S = 0.2\,\Omega$ and $1/R_{sh} = 0$.

Following the work of Kammer *et al.*,[2] we removed illumination, i.e., imposed "dark" conditions, and measured the current in series with a commercial diode when we apply an external voltage, scanning through from reverse bias of -20 V to a forward bias of $+1$ V. The slope in the linear reverse-biased region (before the breakdown voltage is reached) determines the shunt resistance in our equivalent circuit. A similar measurement using the *p-n* junction fabricated at CSUEB by students shows the hallmark rectifying behavior of a diode in the *I* vs. *V* curve as seen in Fig. 6.

V. DISCUSSION OF RESULTS

Figures 4 and 5 allow comparison of the performance of a commercial mini solar panel with a solar cell that students created in the lab. The student-fabricated solar cell indeed demonstrates the photovoltaic effect, producing electrical power; however, the IV curve is suppressed below the classic IV curve of a good commercial grade solar panel. The short-circuit current density J_{SC} for the student-fabricated cell is approximately 25% that of the commercial panel.

Ideally, an efficient solar cell should have a large shunt resistance and a small series resistance. Both types of parasitic resistances can reduce the performance of the solar cell *p-n* junction. A large series resistance will not significantly reduce the V_{OC} of a solar cell, whereas a very small shunt resistance will; this fact provides a simple test to discern which parasitic resistance dominates the inefficiency. As seen in Fig. 5, the V_{OC} remains at about the same value as the commercial cell; thus, students concluded that a large series resistance suppressed the performance of their fabricated cells.

Additionally, fitting the linear section of the reverse-bias region of the "dark" curves in Fig. 6 allows extraction of the shunt resistance, R_{sh}, which we found to be $\sim$1 kΩ for both samples, a value large enough to be considered infinite in the Eq. (1) model without significant effect. While the effects of R_{sh} are not significant, we can reproduce the shape and magnitude of the short-circuit current density, $J_{SC} \cong 1.6\,\mathrm{mA/cm^2}$,

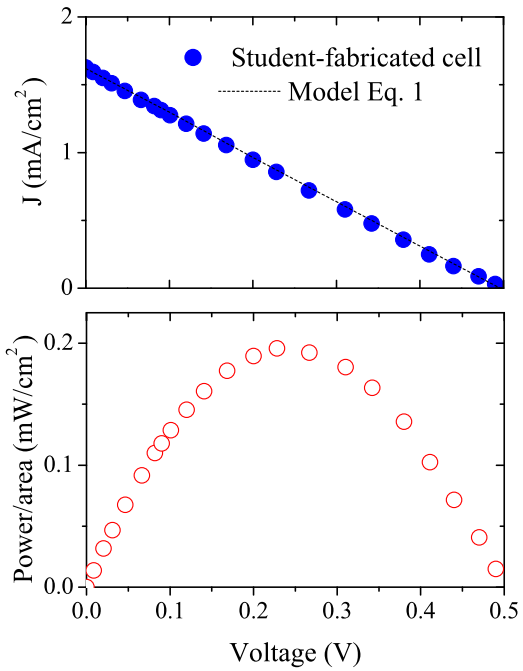

Fig. 5. JV curve for a student-fabricated p-n junction (area 5 cm^2) tested under similar light conditions as the commercial cell, with corresponding power curves. Fit is Eq. (1) using $R_S = 14\,\Omega$ and $1/R_{sh} = 0$.

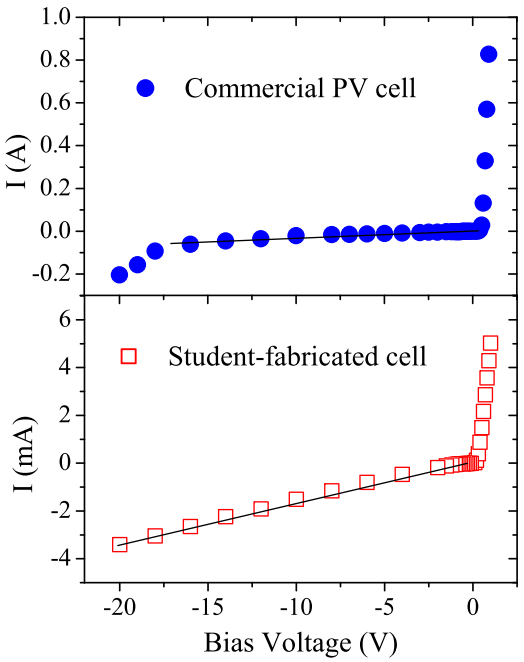

Fig. 6. Forward and reverse bias IV curves under "dark" conditions for the commercial mini panel and the p-n junction fabricated by students at CSUEB. Fitting the linear portion of this curve allows extraction of the shunt resistance as $\sim$1 k Ω for both samples, meaning that low shunt resistance is not limiting the efficiency in either case.

for the fabricated solar cell by including a series resistance $R_S = 14\,\Omega$ in our Eq. (1) model. Additionally, using the variable irradiance method, we measure $R_S \approx 10\,\Omega$ for our fabricated cell, which corroborates our model fit. Our single-parameter IV curve match suggests that while multiple sources likely contribute to the poor performance of the fabricated solar cell, the effects can be summarized in terms of a large series resistance. Series resistance is affected by deep level traps and contact resistance between silicon and metal leads. We suspected that residual Fe from our annealing furnace caused the large series resistance since Fe in Si acts as a deep level trap, which increases the recombination rate of carriers.[24] Shorter lifetimes of the free carriers leads to lower conductivity, hence higher series resistance. Confirming this claim, we measured the Fe concentration in our annealed samples using Secondary Ion Mass Spectrometry (SIMS) to be $\sim 10^{16}$ atoms/cm^3, which is a sufficient density to significantly shorten carrier lifetimes, thus degrading collection efficiency.

VI. CONCLUSION

We have presented a strategy for student engagement in the fabrication and electrical characterization of *p-n* junction silicon solar cells. Students can gain exposure to a wide variety of research-relevant techniques including, but not limited to: spin coating, dopant diffusion through annealing, chemical etching, thermal evaporation, four-point probe, ellipsometry, and IV electrical characterization. In addition, several physical models are introduced that develop a quantitative framework for visualizing nanometer-scale features. While the performance of the fabricated solar cell was significantly reduced compared to a commercial solar cell, the students were able to fabricate a *p-n* junction that displayed both the photovoltaic effect and classic diode rectification behavior. Students were also able to deduce that the largest contribution to this reduced performance was a large parasitic series resistance.

This lab generates much discussion and interest about the science of solar photovoltaic cells, an important modern-day source of electrical power. Students reported excitement and increased interest in semiconductor physics as a result of this lab. For example, students unanimously reported in surveys an increase in interest in semiconductor technology and excitement for performing the lab again. A site visit to a cleanroom facility as a part of the process, while not necessary, provides students with perspective and insight about how nanoscale technologies are researched and fabricated.

ACKNOWLEDGMENTS

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APPENDIX: EQUIPMENT FOR FABRICATION AND CHARACTERIZATION

1. Fabrication equipment

We summarize the equipment used for the three main fabrication steps and suggest alternatives that may be found in nearby engineering or materials science departments:

Step	Equipment used	Alternative
Spin-coating	Laurell Technologies spin coater	Home-made using CPU cooling fan.[16]
Annealing	Lindberg/Blue box furnace (non-vacuum)	Standard tube furnace (use small pieces, cleave after annealing)
Etch	6:1 Buffered oxide etch (BOE) dip. **Note: Use extreme caution! HF is dangerous!**	Other HF concentrations possible.

2. Characterization equipment:

- Light source—65 W lamp (or the sun)
- Commercial solar mini panels (0.45 V, 400 mA; Pitsco Education, $5 each) for calibration
- Decade resistor box (or range of resistors, 0.1–200 Ω)
- Multimeter—10 μA or 1 mV precision (e.g., Agilent 34401A DMM or Fluke model 116 handheld DMM)
- Optional:
  - Four-probe: current / voltage source (e.g., Keithley 2401 Sourcemeter), four-point test probes
  - Ellipsometry: J.A. Woollam alpha-SE spectroscopic ellipsometer

We are glad to offer course materials to instructors interested in bringing this lab to their institute; please contact us through the CSUEB Physics Department webpage.

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Weeden Steam Engine Model

Prior to the reform of high school physics texts ca. 1960 there was a fair amount of technology in the secondary school curriculum. Many texts included pictures of the workings of a steam engine, and schools often had steam engine models. The Weeden #32 stationary steam engine in the picture came to my collection from a local high school, and I have often wondered if it was a Christmas present that found its way there. This "Eureka" model was introduced in 1896 and was made until 1927. The water in the boiler could be heated either electrically or with solid fuel. Note the vertical sight glass on the left-hand side to keep track of the water level in the boiler. (Picture and Notes by Thomas B. Greenslade, Jr., Kenyon College)