Experimental High Speed CMOS Image Sensor System and Applications

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Abstract

CMOS image sensors are capable of very high-speed non - destructive readout, enabling many novel applications. To explore such applications, we designed and prototyped an experimental high speed imaging system based on a CMOS digital pixel sensor (DPS). The experimental system comprises a PCB that has the DPS chip interfaced to a PC via three I/O cards supported by an easy to use software environment. The system is capable of image acquisition at rates of up to 1,400 frames/sec. After describing the DPS chip and experimental imaging system,we present two applications: dynamic range extension and optical flow estimation. These applications rely on the DPS's ability to perform non-destructive readout of multiple frames at high-speed.

Keywords

Image sensors, imaging, dynamic range, FPN.

INTRODUCTION

CMOS image sensors are capable of very high speed non - destructive readout [1, 2, 3]. This capability and the potential of integrating memory and signal processing with the sensor on the same chip enable the implementation of many new still and video rate image processing applications at low cost and power consumption [4].

To explore such applications, we designed and prototyped an experimental PC-based high speed CMOS imaging system around the high speed CMOS Digital Pixel Sensor (DPS) chip designed by our group [3]. The DPS chip comprises 352×288 pixels, each containing a photogate circuit, a comparator, and 8 3T-DRAM cells, and is fabricated in a standard 0.18μm CMOS technology. The chip performs "snap-shot" image acquisition, pixel-parallel 8-bit single-slope A/D conversion, and digital readout at continuous rate of up to 10,000 frames/s (1 Gpixels/s). The experimental system comprises a PCB interfaced to a PC via three I/O cards supported by an easy to use software environment. It is capable of image acquisition at rates of up to 1,400 frames/s, which, although slower than the maximum frame rate of the chip, is high enough for the intended applications. In the following section we briefly describe the the DPS chip. Then, we describe the experimental imaging system, and finally, we present experimental results that demonstrate the use of high speed imaging in still and video rate applications. The first application we demonstrate is dynamic range extension via multiple capture. In addition to using saturation detection, which extends dynamic range at the high illumination end, we explore the use of a recently proposed method for high dynamic range motion blur free imaging [5, 6]. The second application is the use of a high speed video sequence to accurately estimate optical flow and to perform gain FPN correction [7, 8].

DPS CHIP

A complete description of the chip and testing results has been reported in [3]. For completion, we provide a brief description of the design in this section. The main chip characteristics are provided in Table 1, and a pixel schematic is given in Figure 1. Each pixel consists of an nMOS photogate, a transfer gate, reset transistor, a storage capacitor, and an 8-bit single-slope ADC with an 8-bit 3T-DRAM. The photogate subcircuit uses thick oxide (3.3V) transistors available for use in the chip I/O cells to combat the high gate and subthreshold leakage currents and the low supply voltage problems of the 1.8V thin oxide transistors. The rest of the circuit uses thin oxide transistors to minimize area and power. The comparator consists of a differential amplifier stage followed by two single-ended gain stages. It is designed to provide 10-bits of resolution at an input swing of 1V and worst case settling time of 80ns. This provides the flexibility to perform 8-bit A/D conversion down to 0.25V swing in 25μs, which is needed for high-speed operation and under low light conditions. The 3T-DRAM is designed for a maximum data hold time of 10ms. Single-ended charge-redistribution column sense-amps are used to achieve robustness against voltage coupling between the closely spaced bit lines. The comparator and pixel-level

memory circuits can be tested completely electrically by applying analog signals to the sense node through the "Reset Voltage" signal, performing A/D conversion and reading out the digitized values.

Table 1. Chip characteristics [3].

Technology	0.18μm 5-metal CMOS
Die size	5×5 mm
Array size	352×288 pixels
Number of transistors	3.8 million
Readout architecture	64-bit (167 MHz)
Max output data rate	>1.33 GB/s
Max continuous frame rate	>10,000 frames/s
Max continuous pixel rate	>1 Gpixels/s
Pixel size	9.4×9.4μm
Photodetector type	nMOS Photogate
Number of transistors/pixel	37
Sensor fill factor	15%

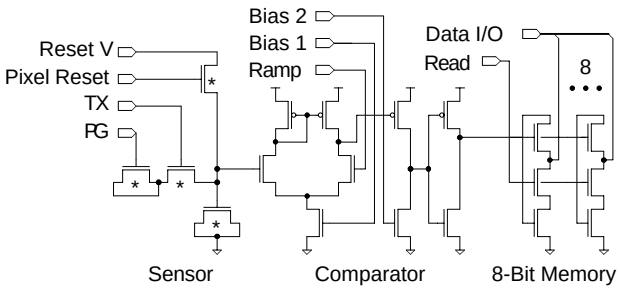


Figure 1. DPS Pixel Schematic (Stars indicate thick oxide transistors).

A block diagram of the DPS chip is shown in Figure 2. The core is a 352 × 288 pixel array. The input-related periphery consists of an 8-bit gray code counter, column drivers and multiplexers. Control periphery includes row-select pointer for addressing the pixel-level memory, comparator power down circuits, and timing control and clock generation circuits. Output periphery includes column sense-amps for reading the pixel-level memory, and an output for multiplexing shift register.

The ADC operation is illustrated in Figure 3. A globally distributed voltage ramp is connected to each pixel's comparator inverting input. The non-inverting input of each comparator is directly connected to the storage capacitor (sense node) of the pixel. At the beginning of conversion, the voltage ramp is set to the lowest expected voltage of the sense node, which sets the comparator output to high. A globally distributed internally generated gray code is continuously loaded to the 8-bit DRAM. As soon as the voltage ramp crosses the sense node voltage, the comparator switches and the final gray code before switching stays stored in the DRAM. Alternatively, a digital ramp sequence that is generated off-chip can be used instead of the internally generated gray code, allowing other conversion strategies such as logarithmic compression and expansion.

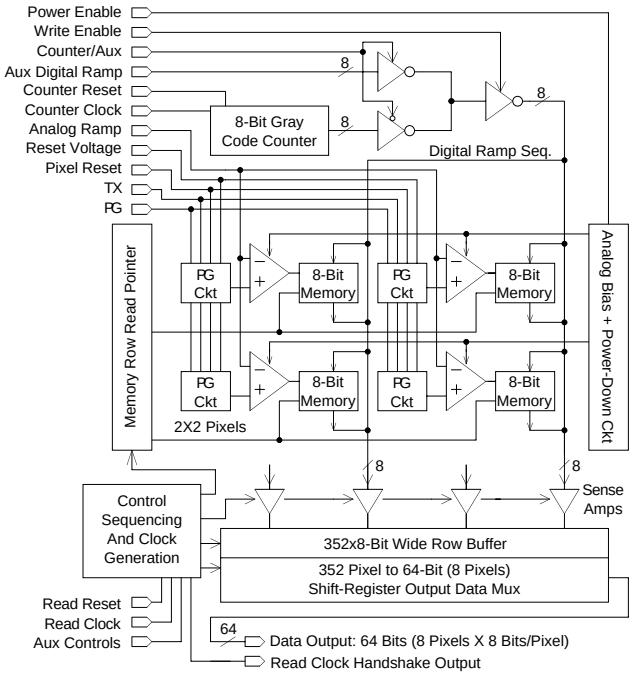


Figure 2. Block Diagram of the DPS Chip.

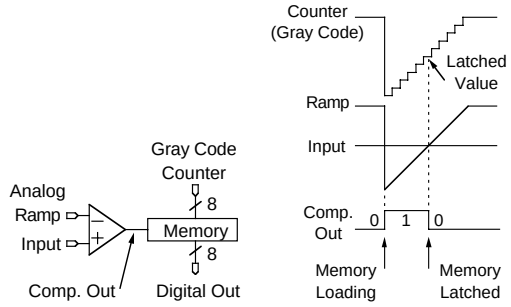


Figure 3. Single-slope ADC operation.

The pixel values are read out of the memory one row at a time using the read row-pointer and column sense-amps. Each row is then shifted out, while the next row is read out of the memory. To reach over 1 Gigapixels/second throughput a 64-bit-wide readout bus operating at 167 MHz is used. The readout operation is coordinated by on-chip control logic operating off of a frame reset strobe and a single clock. Since the design allows full-frame conversion and readout to be accomplished in under 100μs, average power consumption may be significantly reduced when operating the sensor at lower speeds by powering down the comparators. This is accomplished using on-chip digitally controlled power-down circuits.

The operation of the imager can be divided into four phases: reset, integration, A/D conversion and readout. The reset, integration and A/D conversion all occur in parallel over the entire array ("snap-shot" mode), which avoids the image

distortion due to row-by-row reset and readout of APS. To minimize the charge injection to the sense node during pixel reset, a slow falling edge for the pixel reset must be used; this requires analog conditioning of the reset signal. The operation of the DPS imager is also quite flexible. One can arrange the above-mentioned four phases in any order and can perform read and integration in parallel. Figure 4 illustrates two such schemes, namely for multi-capture and for video mode with digital CDS (Correlated Double Sampling).
The DPS characterization results obtained from an initial testing setup ([3]) are listed in Table 2.

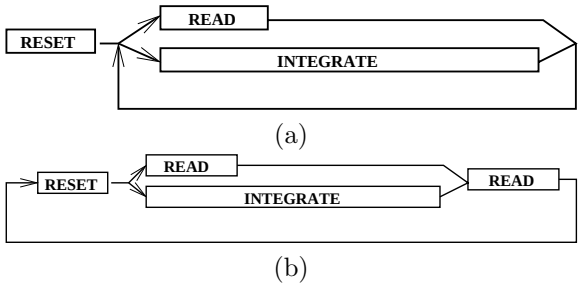


Figure 4. DPS operation schemes: (a) Multi-capture, and (b) Video mode with correlated double sampling.

Table 2. DPS imager characterization results [3]. All numbers, except for power consumption are at 1000 frames/s.

Power used at 10K fps	50mW, typical
ADC architecture	Per-pixel single-slope
ADC resolution	8-bits
ADC conversion time, typical	$\sim$25μs, ($\sim$20μs, min.)
ADC range, typical	1V
ADC integral nonlinearity	$<$0.22% (0.56 LSB)
Dark current (20^{o}C)	130mV/s, 10nA/cm^2
Quantum efficiency	13.6%
Conversion gain	13.1μV/e$^-$
Sensitivity	0.107V/lux.s

EXPERIMENTAL SETUP

We set up an experimental system based on the DPS chip described in the previous section to explore applications of high speed non-destructive readout to still and video imaging. The experimental system comprises a PCB interfaced to a PC via three 20MHz 32-bit National Instrument I/O cards (Figure 5). The PCB we designed, which houses the DPS chip, provides the analog and digital signals needed to operate the chip and interface its 64-bit wide output bus to the I/O cards. Front end optics is provided by attaching a metal box with a standard C-mount lens to the PCB. The system is software programmable through a MATLAB interface.

We decided to use three I/O cards instead of one or two higher speed ones for simplicity, robustness and maximum interface

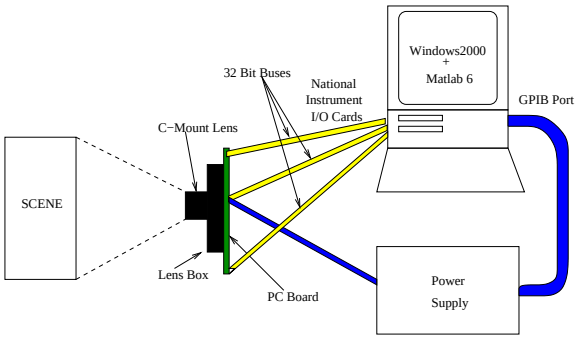


Figure 5. The experimental imaging setup.

flexibility. One of the boards is used to send control data to the board, while the others are used to grab the imager data, 64 bits per clock cycle. This system achieves frame rates of up to 1400 frames/s. Although this is slower than the 10,000 frames/s capability of the DPS chip, it is high enough for the intended applications.
The photograph of one side of the PCB with different areas labeled is shown in Figure 6. The control port on the left side provides signals from the PC to control the clock generator, analog signal generators, clock gates and the DPS imager. The analog signals such as ADC ramp, pixel reset, biases to the pixel array and sense-amps are generated on the board via DACs, op-amps, and simple potentiometers.
To simplify the software interface, we implemented a MATLAB function toolbox that provides the user with high level commands with inputs such as total exposure time and number of captures, to program the desired acquisition. For example to acquire a video sequence with CDS, the following code may be used:

```
ca = pdccamera;
set(ca,'Exposure',[0 ExposureTime]);
for j=1:NumberOfFrames
   start(ca);
   image = getData(ca);
end
clear(ca);
```

For multiple non-destructive (i.e., with no intermediate resets) capture the following code is used:

```
ca = pdccamera;
set(ca,'Exposure',[0 ExpTime1 ExpTime2 ...
ExpTimeN]);
start(ca);
image = getData(ca);
clear(ca);
```

We used the system to characterize sensor FPN, temporal noise and ADC characteristics. Results are shown in Table 3 and Figure 7. For the FPN and temporal noise characterization, digital CDS subtraction was performed before the noise values were calculated. For ADC characterization, the electrical testability feature of the DPS chip was used.

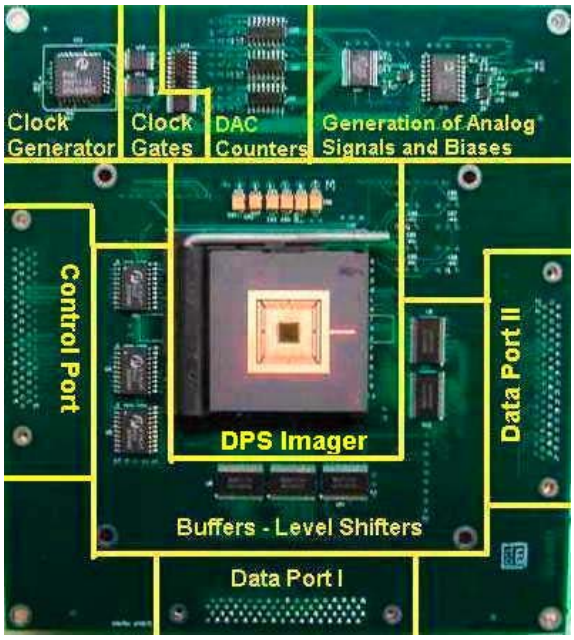


Figure 6. The PCB supporting the DPS chip.

Table 3. DPS imager characterization summary, with the experimental setup shown in Figure 5 (The light measurements were taken at 30% of saturation at 0.5V swing).

FPN, w/light, CDS	1.2 LSB
FPN, dark, CDS	0.28 LSB
Temporal noise, w/light, CDS (20^{o}C)	1.1 LSB
Temporal noise, dark, CDS (20^{o}C)	0.75 LSB

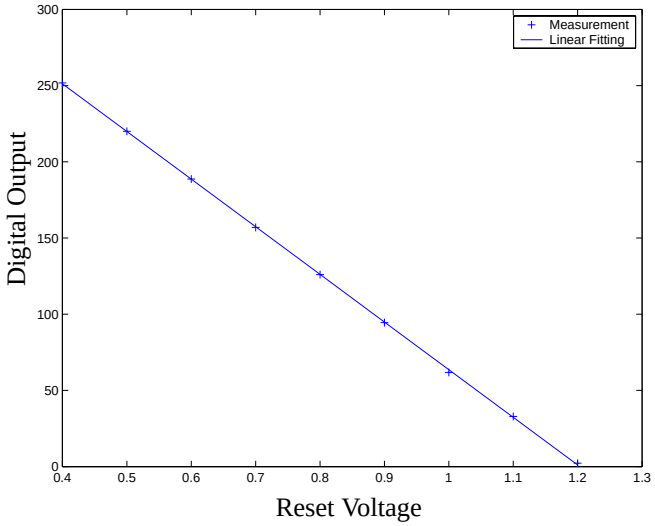


Figure 7. Characteristics of sensor ADC's.

APPLICATIONS

In this section we provide experimental results that demonstrate two applications of the high-speed system: one application is for still and a second for video imaging.

Dynamic Range Extension

An algorithm for synthesizing a high dynamic range, motion blur free, still image from multiple captures was previously presented in [5, 6]. The algorithm consists of two main procedures, photocurrent estimation [5] and motion/saturation detection [6]. Estimation is used to reduce read noise and thus to enhance dynamic range at the low illumination end. Saturation detection is used to enhance dynamic range at the high illumination end, while motion blur detection ensures that the estimation is not corrupted by motion. Motion blur detection also makes it possible to extend exposure time and to capture more images, which can be used to further enhance dynamic range at the low illumination end. The algorithm operates locally; each pixel's final value is computed using only its captured values. The algorithm also operates recursively, requiring the storage of only a constant number of values per pixel independent of the number of images captured. These modest computation and storage requirements make the algorithm well suited for single chip digital camera implementation.

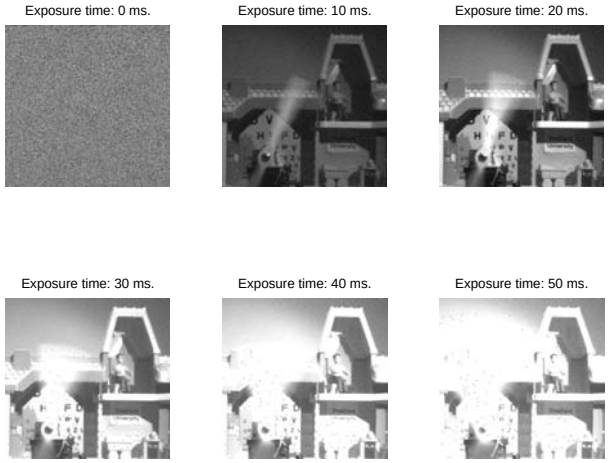
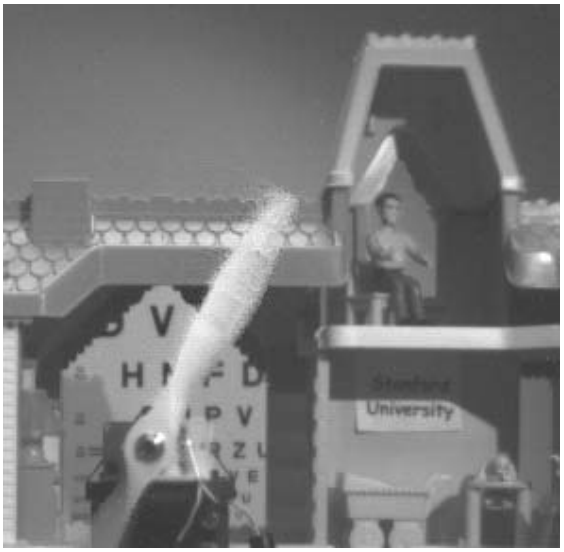


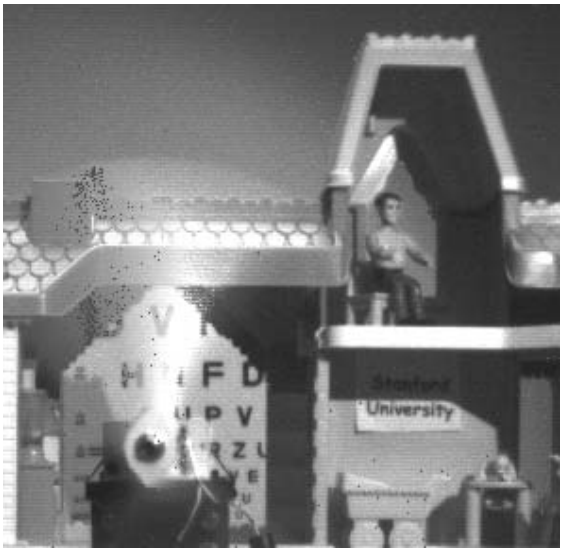
Figure 8. Examples of non-destructively captured images at 1000 frames/s. 65 frames over a total of 64ms are captured.

The high dynamic range scene used in the experiment comprised a doll house under direct illumination from above and a rotating model airplane propeller. We captured 65 frames of the scene at 1,000 frames/s non-destructively and uniformly spaced over a 64ms exposure time. Figure 8 shows some of the images captured. Note that as exposure time increases, the details in the shadow area (such as the word "Stanford") begin to appear while the high illumination area suffers from saturation and the area where the propeller is rotating suffers from significant motion blur.

Figure 9 (a) shows the high dynamic range, motion blur free image synthesized from the 65 captures using the algorithm discussed in [6]. Note that the dark background is much smoother due to reduction in readout noise and FPN, and the motion blur caused by the rotating propeller is almost completely eliminated. The high dynamic range image constructed with the same captures but with the last sample before saturation algorithm [9] is also shown in Figure 9 (b).



(a)

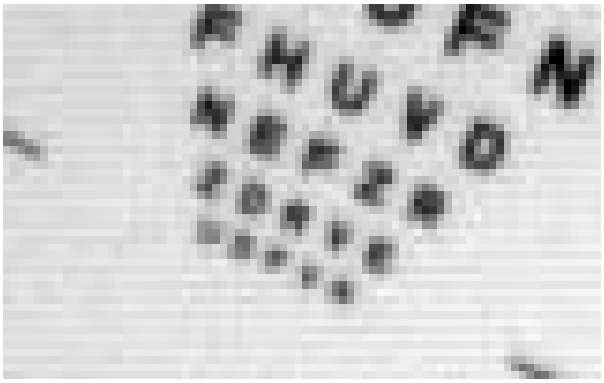


(b)

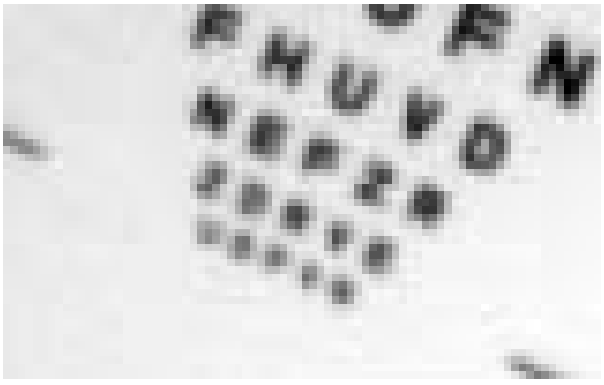
Figure 9. High DR images constructed from 65 multiple captures: (a) Motion blur free image (b) Image generated with last sample before saturation algorithm [9].

Optical flow estimation and gain FPN correction

In [4, 7] it was shown that the high speed imaging capability of CMOS image sensors can be used to obtain more accurate optical flow with wide range of scene velocities in real time and without unduly increasing the off-chip data. The method described finds high accuracy optical flow at a standard frame rate (e.g., 30 frames/s) using a high frame rate sequence. The Lucas-Kanade method is used to obtain optical flow estimates at the high frame rate, which are then accumulated and refined to obtain the optical flow estimates at the standard frame rate. The accurate optical flow estimates can then be used to perform a wide variety of tasks ranging from video compression to 3D structure estimation and superresolution. Optical flow can also be used to correct imager gain FPN as was presented in [8]. The algorithm assumes that brightness along the motion trajectory is constant over time. The pixels are grouped in blocks (typically 5×5) and each block's pixel gains are estimated by iteratively minimizing the sum of the squared brightness variations along the motion trajectories.



(a)



(b)

Figure 10. Correlated double sampled images from camera: (a) with gain FPN (b) without gain FPN.

To demonstrate the gain FPN algorithm proposed in [8], we used our system to capture 12 frames of an eye chart at 200 frames/sec. We then used the algorithm in [7] to estimate optical flow. Finally, we used the sequence and the estimated optical flow to correct gain FPN. Figure 10

(a) shows one of the frames from the captured sequence and Figure 10 (b) shows the same frame after correcting the gain FPN. By comparing the two figures, we can see that the non-uniformity resulting from gain FPN has been removed without blurring the image. Note that in this application both spatial and temporal information are used to enhance the image quality whereas only temporal information is used when synthesizing a high dynamic range image.

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