

# Yao Hsiao

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## Education

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### Stanford University

M.S / Ph.D. in Electrical Engineering, GPA: 4.1/4.3

Stanford, CA  
Jun. 2023 / Sep. 2021 - Present

### National Tsing Hua University

B.S. in Electrical Engineering, GPA: 4.22/4.3

Phi Tau Phi Scholastic Honor, rank: 1/112

Hsinchu, Taiwan  
Sep. 2016 – Jun. 2020

## Research Interest

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- Computer architecture – Microarchitecture, Concurrency, Memory Systems, Hardware Security
- Formal Verification

## Experience

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### Stanford University

Research Assistant, Prof. Caroline Trippel's group

Stanford, CA

Jul. 2020 – Present

- Researched in methodology for verifying hardware compliance to state-of-art defenses against hardware side-channel attacks
  - Developed novel abstraction that enables efficient verification of side-channel defenses against hardware implementation and provides a unifying formal framework in reasoning about hardware side-channel attacks
  - Designed the first automatic tool for characterizing side-channels on hardware designs to provide leakage specification that reflects hardware reality and provides information required for hardware and software defenses, deployed it on complex RISC-V processor core featuring speculation and out-of-order write-back, and uncover novel side-channel leakage
- Developed automated methodology for synthesizing formal models from RTL to enable verification of Memory Consistency Model (MCM) implementation, a key aspect of modern multiprocessors, deployed it on four-core multi-V-scale to attain the first complete proof on its MCM implementation correctness, thus advancing the state-of-art

### Apple Inc.

Research Intern, CPU Formal Verification team

Cupertino, CA

Jun. 2022 – Sep. 2022

- Developed automated tool for synthesizing formal models of hardware proven upheld by the RTL design to enable efficient verification of RTL compliance to hardware-software contracts, and showed effectiveness on real-world RTL designs

### Apple Inc.

Research Intern, CPU Formal Verification team

Cupertino, CA

Jun. 2021 – Aug. 2021

- Proposed roadmap in developing tools that auto-generate properties for formal verification, and formulated abstraction on RTL design and integrated Verific front-end parser into synthesis tool for dataflow analysis as first steps
- Conducted experiment on the proposed methodology and attained results highly similar to manually crafted properties

### Academia Sinica, Institute of Information Science

Research Assistant, Dr. Yu-Fang Chen's group

Taipei, Taiwan

Jan. 2020 – Aug. 2020

- Revised an SSD emulator and a file system with a new disk model to attain 30x performance over the original xv6
- Designed optimization for a system through analysis and expertise in cache design and attained 1.4x performance

## Publications

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- **Yao Hsiao**, Nikos Nikoleris, Artem Khyzha, Dominic P. Mulligan, Gustavo Petri, Christopher W. Fletcher, and Caroline Trippel. "RTL2M $\mu$ PATH: Multi- $\mu$ PATH Synthesis with Applications to Hardware Security Verification". In Proceedings of the 57th International Symposium on Microarchitecture (MICRO), November 2024. Acceptance rate: 113/497=22.7%
- **Yao Hsiao**, Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri, and Caroline Trippel. "Synthesizing Formal Models of Hardware from RTL for Efficient Verification of Memory Model Implementations". In Proceedings of the 54th International Symposium on Microarchitecture (MICRO), October 2021. Acceptance rate: 94/421=22.3%
- Yun-Sheng Chang, **Yao Hsiao**, Tzu-Chi Lin, Che-Wei Tsao, Chun-Feng Wu, Yuan-Hao Chang, Hsiang-Shang Ko, and Yu-Fang Chen. "Determinizing Crash Behavior with a Verified Snapshot-Consistent Flash Translation Layer". In Proceedings of the 14th USENIX Symposium on Operating Systems Design and Implementation (OSDI), Nov. 2020. Acceptance rate: 70/400=17.5%

## Presentations

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- "RTL2M $\mu$ PATH: Multi- $\mu$ PATH Synthesis with Applications to Hardware Security Verification". **Yao Hsiao**, Nikos Nikoleris, Artem Khyzha, Dominic P. Mulligan, Gustavo Petri, Christopher W. Fletcher, and Caroline Trippel. Intel Scalable Assurance Annual Workshop. Sep, 2024.

- "Scalable Assurance via Verifiable Hardware-Software Contracts". **Yao Hsiao**. Academia Sinica, Taipei. Jan, 2024.
- "Design for Hardware Memory Model Verification". **Yao Hsiao**, Yasas Seneviratne, Tommy Tracy II, Kevin Skadron, Caroline Trippel. Programming Languages for ARCHitecture (PLARCH) 2023 Workshop (co-located with ISCA23). Jun. 2023.
- "Formal Characterization of Hardware Transmitters for Secure Software and Hardware Repair". **Yao Hsiao**, Christopher Fletcher, Caroline Trippel. The Fifth Young Architect Workshop (co-located with ASPLOS23). Mar. 2023.
- "Scalable Assurance via Verifiable Hardware-Software Contracts". **Yao Hsiao**, Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri and Caroline Trippel. Open-Source Computer Architecture Research workshop (co-located with ISCA 2022). Jun. 2022.
- "Synthesizing Formal Models of Hardware from RTL for Efficient Verification of Memory Model Implementations". **Yao Hsiao** Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri and Caroline Trippel. 7th Career Workshop for Inclusion and Diversity in Computer Architecture workshop. Oct. 2021.
- "Lifting Axiomatic Hardware Specifications from RTL for Security Analysis". **Yao Hsiao** and Caroline Trippel. 6th Career Workshop for Women & Minorities in Computer Architecture. Oct. 2020.

## Mentoring

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**Kaia Li**

*Jun, 2024 - Present*

Stanford University M.S. expected 2025

- Kaia is working on execution contract verification crucial for defenses against speculative execution attacks such as Spectre.

## Awards and Honors

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- Apple Stanford EE PhD Fellowship in Integrated Systems (full tuition and stipend support for year 2024-2025)
- Microarchitectural Attacks and Defenses (MAD) Workshop Capture the Flag Contest: 1st place with prize received
- Stanford Electrical Engineering Department Fellowship for PhD Student
- NTHU Dean's List Award – 2016 Fall, 2017 Spring, 2018 Spring, 2018 Fall, 2019 Spring, 2019 Fall, 2020 Spring

## Projects

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**Adaptive Routing Exploiting Temporal Locality of Traffic (Final Project for Interconnection Network)** *Stanford., CA*

Team Leader

*Jan. 2022 – Mar. 2022*

- Designed traffic predictor to predict near-future traffic, incorporated the predictor into a minimal adaptive routing for mesh with dateline approach as deadlock avoidance, and evaluated the scheme against different routing algorithms

**Graph Partitioning Hardware Design**

*Hsinchu, Taiwan*

Team Leader

*Dec. 2019 – Jan. 2020*

- Led a 3-person team to design specialized parallel hardware for graph partitioning and implement from RTL design, synthesis, to place-and-routing with over 16x speedup in total throughput compared to sequential pipeline version
- Devised architecture design including memory banking schemes coupled with customized computation units and a novel FIFO circuit with variable data come-in rates to achieve a balance in both latency (16x) and area (128x)

**A Study on Smooth Particle Hydrodynamics (SPH) Method**

*Hsinchu, Taiwan*

Team Leader

*Jan. 2020*

- Analyzed SPH method for parallel computing and time complexity, devised 9.7x speedup schemes for SPH method on single GPU compare to single threaded version, and conducted profiling to identify bottleneck in memory coalescing

## Teaching

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**Stanford University**

*Palo Alto, CA*

Course Assistant for EE 282 – Computer Systems Architecture

*2024 Spring*

- Designed written and programming assignments, held office hours, managed logistics, helped designing and grading exams

**National Tsing Hua University**

*Hsinchu, Taiwan*

Teaching Assistant for EE 3450 – Computer Architecture

*2019 Fall*

- Designed programming assignments on RISC-V ISA to improve course quality and assisted students in materials

## Technical Skills

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- Language: C/C++, Python, SystemVerilog/Verilog & SytemVerilog Assertion, RISC-V assembly, Bash, Tcl, Alloy
- Softwares & Libraries: Cadence JasperGold, Verific, Yosys, gem5, BookSim, CUDA, OpenMP, SystemC,

## Relevant Coursework

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- **Stanford University**: Formal Methods on Computer Systems, Computer Systems Architecture, Introduction to VLSI Systems, Interconnection Networks, Program Analysis and Optimizations, Programming Language, Introduction to Computer Networks, Parallel Processors Beyond Multicore Processing, Information Theory, Decision Making under Uncertainty