Yao Hsiao

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Education

Stanford University *Stanford, CA*
M.S / Ph.D. in Electrical Engineering, GPA: 4.1/4.3 Jun. 2023 / Sep. 2021 - Present (Expected Jun. 2026)
- Advisor: Prof. Caroline Trippel
- Thesis (Working Title): Multi-μPATH Synthesis with Applications to Hardware Concurrency and Security Verification

National Tsing Hua University *Hsinchu, Taiwan*
B.S. in Electrical Engineering, GPA: 4.22/4.3 Sep. 2016 – Jun. 2020
Phi Tau Phi Scholastic Honor, rank: 1/112

Awards and Honors

- 2025 Top Picks in Hardware and Embedded Security finalist (final award TBD) for RTL2MμPATH
- Apple Stanford EE PhD Fellowship in Integrated Systems (full tuition and stipend support for year 2024-2025)
- Microarchitectural Attacks and Defenses (MAD) Workshop Capture the Flag Contest: 1st place with prize received
- Stanford Electrical Engineering Department Fellowship for PhD Student
- NTHU Dean's List Award - 2016 Fall, 2017 Spring, 2018 Spring, 2018 Fall, 2019 Spring, 2019 Fall, 2020 Spring
- 2019 MOST Collegiate Research Scholarship – A study on accelerator design for neural network using FPGA and HLx
- 2018 McKinsey Scholar Program – A selected group of students invited for management consulting training and mentorship

Publications

- **Yao Hsiao**, Nikos Nikoleris, Artem Khyzha, and Caroline Trippel. "Consistency-Directed Formal Verification of Cache Coherence Protocol Implementations". In preparation.
- **Yao Hsiao***, Yasas Nayomal Seneviratne*, Tommy Tracy, Kevin Skadron, and Caroline Trippel. "Blended Formal and Runtime Verification for Unbounded Hardware Proofs with Applications to Memory Consistency Model Verification". In preparation. *Equal contribution.
- **Yao Hsiao**, Nikos Nikoleris, Artem Khyzha, Dominic P. Mulligan, Gustavo Petri, Christopher W. Fletcher, and Caroline Trippel. "RTL2MμPATH: Multi-μPATH Synthesis with Applications to Hardware Security Verification". In Proceedings of the 57th International Symposium on Microarchitecture (MICRO), November 2024. Acceptance rate: 113/497=22.7%
- **Yao Hsiao**, Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri, and Caroline Trippel. "Synthesizing Formal Models of Hardware from RTL for Efficient Verification of Memory Model Implementations". In Proceedings of the 54th International Symposium on Microarchitecture (MICRO), October 2021. Acceptance rate: 94/421=22.3%
- Yun-Sheng Chang, **Yao Hsiao**, Tzu-Chi Lin, Che-Wei Tsao, Chun-Feng Wu, Yuan-Hao Chang, Hsiang-Shang Ko, and Yu-Fang Chen. "Determinizing Crash Behavior with a Verified Snapshot-Consistent Flash Translation Layer". In Proceedings of the 14th USENIX Symposium on Operating Systems Design and Implementation (OSDI), Nov. 2020. Acceptance rate: 70/400=17.5%

Experience

Stanford University *Stanford, CA*
Research Assistant, Prof. Caroline Trippel's group Jul. 2020 – Present
- Developed automated and scalable tools for formally verifying processor implementations of cache coherence, memory consistency, and side-channel security features, by leveraging a novel formal microarchitectural abstraction
- Deployed these tools on open-sourced and commercial hardware (Murφ/RTL), finding bugs and underspecifications

Apple Inc. *Cupertino, CA*
Research Intern, Platform Architecture team Jun. 2025 – Sep. 2025
- Developed and merged new features into a large-scale C++ simulator for improving memory subsystem performance
- Synthesized insights informative for future design directions, identified existing redundancy and optimization opportunities, and achieved up to 5% improvement for selected workloads via an end-to-end design space exploration

Apple Inc. *Cupertino, CA*
Research Intern, CPU Formal Verification team Jun. 2022 – Sep. 2022
- Developed a formal hardware memory consistency model verification tool, which avoids manual property writing and significantly outperforms (in runtime and scalability) traditional verification approaches

Apple Inc. *Cupertino, CA*
Research Intern, CPU Formal Verification team Jun. 2021 – Aug. 2021
- Proposed a roadmap for developing tools that automated difficult verification tasks and implemented the first phase: developed a novel formal hardware abstraction to guide verification, integrated the Verific Verilog parser into a synthesis tool for dataflow analysis, and showed the proposed methodology to be promising with a not-then-automated prototype

National Tsing Hua University *Hsinchu, Taiwan*
Research Assistant, Prof. Jing-Jia Liou's group Feb. 2020 – Aug. 2020

- Designed code generation for a customized accelerator architecture, optimized memory and computation compiler passes, and automated kernel exploration by integrating an electronic system level simulator into TVM toolchains

Academia Sinica, Institute of Information Science *Taipei, Taiwan*
Research Assistant, Dr. Yu-Fang Chen's group Jan. 2020 – Aug. 2020

- Revised an SSD emulator and a file system with a new disk model to attain up to 30x performance over the original xv6
- Leveraged the new disk model's crash consistency guarantees to attain a 1.4x performance gain for a journaling file system

Presentations

- "RTL2MμPATH: Multi-μPATH Synthesis with Applications to Hardware Security Verification". **Yao Hsiao**, Nikos Nikoleris, Artem Khyzha, Dominic P. Mulligan, Gustavo Petri, Christopher W. Fletcher, and Caroline Trippel. Top Picks in Hardware and Embedded Security Workshop (co-located with ICCAD 2025). Oct. 2025.
- "Automatically Uncovering Hardware Side-Channels in Processor RTL with Multi-μPATH Synthesis". **Yao Hsiao**, Nikos Nikoleris, Artem Khyzha, Dominic P. Mulligan, Gustavo Petri, Christopher W. Fletcher, and Caroline Trippel. Open-Source Computer Architecture Research (OSCAR) Workshop (co-located with ISCA 2025). Jun. 2025.
- "RTL2MμPATH: Multi-μPATH Synthesis with Applications to Hardware Security Verification". **Yao Hsiao**, Nikos Nikoleris, Artem Khyzha, Dominic P. Mulligan, Gustavo Petri, Christopher W. Fletcher, and Caroline Trippel. Intel Scalable Assurance Annual Workshop. Sep, 2024.
- "Scalable Assurance via Verifiable Hardware-Software Contracts". **Yao Hsiao**. Academia Sinica, Taipei. Jan, 2024.
- "Design for Hardware Memory Model Verification". **Yao Hsiao**, Yasas Seneviratne, Tommy Tracy II, Kevin Skadron, Caroline Trippel. Programming Languages for ARCHitecture (PLARCH) 2023 Workshop (co-located with ISCA23). Jun. 2023.
- "Formal Characterization of Hardware Transmitters for Secure Software and Hardware Repair". **Yao Hsiao**, Christopher Fletcher, Caroline Trippel. The Fifth Young Architect (YArch) Workshop (co-located with ASPLOS23). Mar. 2023.
- "Scalable Assurance via Verifiable Hardware-Software Contracts". **Yao Hsiao**, Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri and Caroline Trippel. Open-Source Computer Architecture Research (OSCAR) Workshop (co-located with ISCA 2022). Jun. 2022.
- "Synthesizing Formal Models of Hardware from RTL for Efficient Verification of Memory Model Implementations". **Yao Hsiao** Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri and Caroline Trippel. 7th Career Workshop for Inclusion and Diversity in Computer Architecture (CWIDCA) Workshop. Oct. 2021.

Teaching

Stanford University *Palo Alto, CA*
Course Assistant for EE 282 – Computer Systems Architecture 2024 Spring

National Tsing Hua University *Hsinchu, Taiwan*
Teaching Assistant for EE 3450 – Computer Architecture 2019 Fall
Teaching Assistant for EE 2450 – Embedded System Laboratory 2019 Spring

Projects

Adaptive Routing Exploiting Temporal Locality of Traffic (Final Project for Interconnection Network) *Stanford., CA*
Team Leader Jan. 2022 – Mar. 2022

- Implemented minimal credit-based adaptive routing with the dateline approach for deadlock avoidance in BookSim, added to the scheme a predictor (0.52 of accuracy) for near-future traffic, and profiled the scheme against various routing methods

Graph Partitioning Hardware Design *Hsinchu, Taiwan*
Team Leader Nov. 2019 – Jan. 2020

- Designed specialized parallel hardware for graph partitioning and led implementations in RTL design, synthesis, and place-and-routing with over 16x speedup in total throughput compared to sequential pipeline baseline

A Study on Smooth Particle Hydrodynamics (SPH) Method *Hsinchu, Taiwan*
Team Leader Jan. 2020

- Analyzed the SPH method to assess its time complexity and parallelism, devised a CUDA kernel leveraging tiling and unrolling to achieve a 9.7x speedup on a single GPU, and conducted profiling to show linear scaling

Technical Skills

- Language: C/C++, Python, SystemVerilog/Verilog & SytemVerilog Assertion, Murφ, RISC-V assembly, Bash, Tcl, Alloy
- Softwares & Libraries: Cadence JasperGold, Verific, Yosys, BookSim, gem5, SystemC, CUDA, OpenMP, Xilinx HLx

Relevant Coursework

- **Stanford University**: Formal Methods on Computer Systems, Computer Systems Architecture, Introduction to VLSI Systems, Interconnection Networks, Program Analysis and Optimizations, Programming Language, Introduction to Computer Networks, Parallel Processors Beyond Multicore Processing, Information Theory, Decision Making under Uncertainty