Yao Hsiao

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Education

Stanford University *Stanford, CA*

- M.S / Ph.D. in Electrical Engineering (GPA: 4.1 / 4.3) *Jun. 2023 / Sep. 2021 – Present (Expected Jun. 2026)*
- Coursework: Computer Architecture, Formal Methods, Parallel Processor, Interconnection Networks, VLSI Systems

National Tsing Hua University *Hsinchu, Taiwan*

- B.S. in Electrical Engineering, *Phi Tau Phi Scholastic Honor* (GPA: 4.22 / 4.3, rank: 1 / 122) *Sep. 2016 – Jun. 2020*

Experience

Stanford University *Stanford, CA*

Research Assistant, Prof. Caroline Trippel's group *Jul. 2020 – Present*

- Proposed novel methodology for automating formal verification of cache coherence protocol implementations, addresses shortcomings in prior works, and uncovers new bugs in an existing protocol implementations
- Developed novel hardware-software security contracts to formally specify security vulnerabilities of RTL designs
- Designed τsynth, the first automatic tool for verifying RTL compliance to ISA-level security contracts, applied it on CVA6, a RISC-V core featuring speculation, out-of-order write-back, and L1 data cache, with 26 unsafe instructions automatically uncovered, and identified 4 functional bugs on CVA6 core for which fixes were merged into mainstream
- Devised approaches for synthesizing formal models from RTL and formally verifying correctness of CPU memory consistency model implementation, showing its scalability with complete proof on a multicore RISC-V V-scale processor
- Served as a Teaching Assistant for computer architecture course (EE282), developing materials and providing guidance

Apple Inc. *Cupertino, CA*

Research Intern, Platform Architecture SoC *Jun. 2025 – Aug. 2025*

- Developed and merged new features into a large-scale C++ simulator for improving memory subsystem performance
- Synthesizes insights informative for future design direction, identified existing redundancy and optimization opportunities, and achieved up to 5% improvement for selected workloads via an end-to-end design space exploration

Apple Inc. *Cupertino, CA*

Research Intern, CPU Formal Verification *Jun. 2021 – Aug. 2021/Jun. 2022 – Aug. 2022*

- Developed a tool for semi-automatic synthesis of formal model of hardware proven upheld by the industrial-scale RTL design, enabling verification against system-level specifications without costly RTL simulation and manual efforts
- Formulated abstraction on RTL design and developed tools for dataflow graph analysis on RTL netlist, and evaluated efficacy of proposed abstraction with experiments showing the potential of auto-generation of formal properties

Academia Sinica, Institute of Information Science *Taipei, Taiwan*

Research Assistant, Dr. Yu-Fang Chen group *Jan. 2020 – Aug. 2020*

- Integrated a new design of solid-state drive firmware into the xv6 operating system to reduce costly buffer-flush operations used in log-structured file system and attain 30x performance on database workload over the original xv6

Projects

Cache Coherence Protocol for Heterogenous Architecture *Stanford, CA*

Architect *Jun. 2023 – Aug. 2023*

- Synthesized reports on workloads for heterogenous cache coherence protocol, proposed implementation plan for a novel coherence protocol design, implemented simulation on gem5 to show the proposed protocol feasibility

Adaptive Routing Exploiting Temporal Locality in Interconnection Network in Multiprocessor *Stanford, CA*

Team Leader *Jan. 2022 – Mar. 2022*

- Devised learning algorithm for hardware predictor with temporal locality, added to the BookSim simulator a minimal adaptive router with configurability and deadlock avoidance, and achieved up to 50% performance improvement

Honors & Awards

- Apple Stanford EE PhD Fellowship in Integrated Systems – Academic year 2024/2025, 1-year comprehensive funding
- Microarchitectural Attacks and Defenses (MAD) Workshop Capture the Flag Contest: 1st place
- Stanford Electrical Engineering Department Fellowship for PhD Student, 1-year comprehensive funding

Skills

- **Language:** SystemVerilog/Verilog, SystemVerilog Assertions, C/C++, Python, Tcl, Bash, RISC-V assembly
- **Tools & Library:** Cadence Jasper Apps, Murϕ model checker, Verific, Yosys, BookSim, gem5, SystemC, OpenMP, Docker